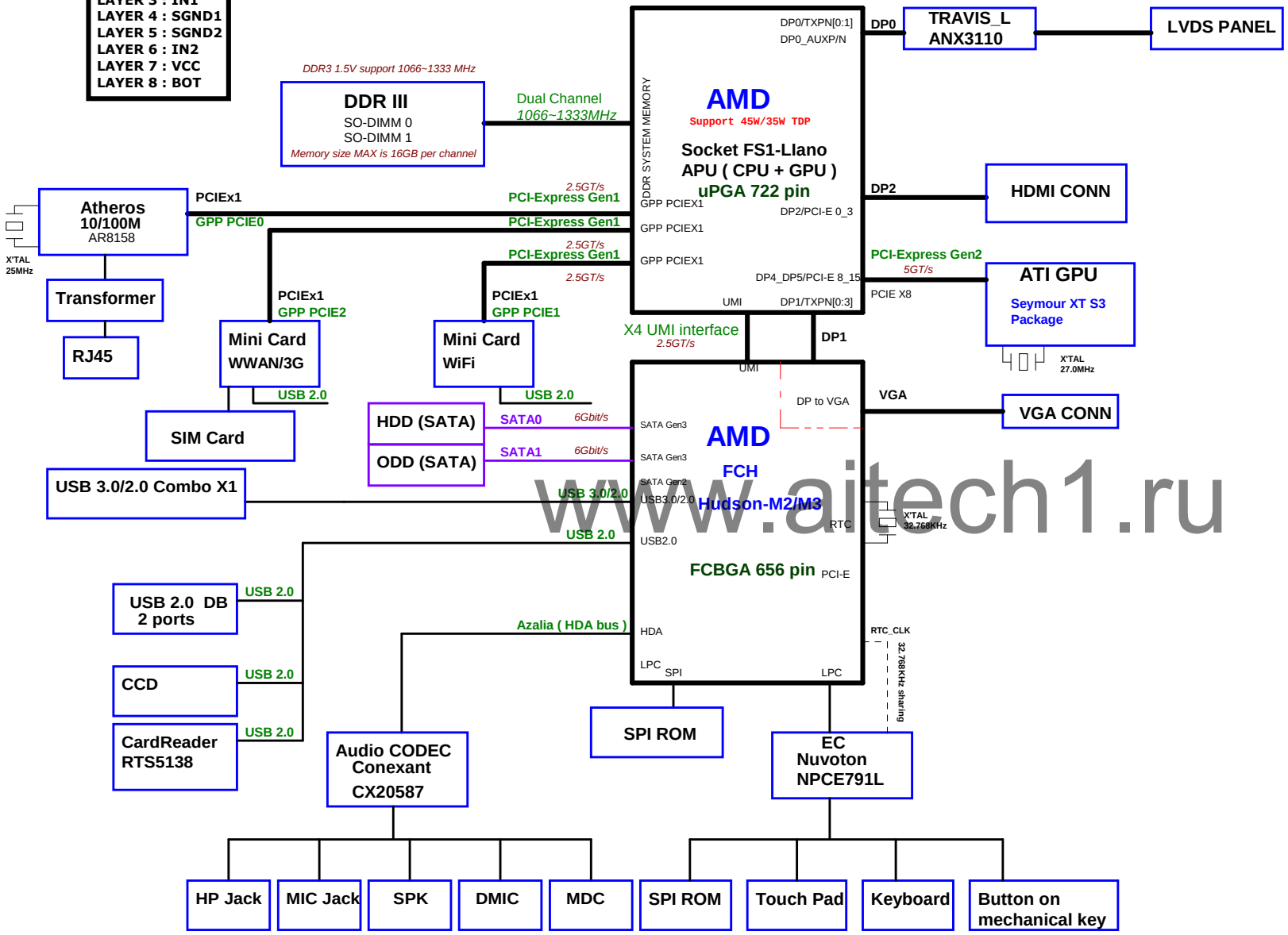
BLOCK DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : SGND1
LAYER 5 : SGND2
LAYER 6 : IN2
LAYER 7 : VCC
LAYER 8 : BOT

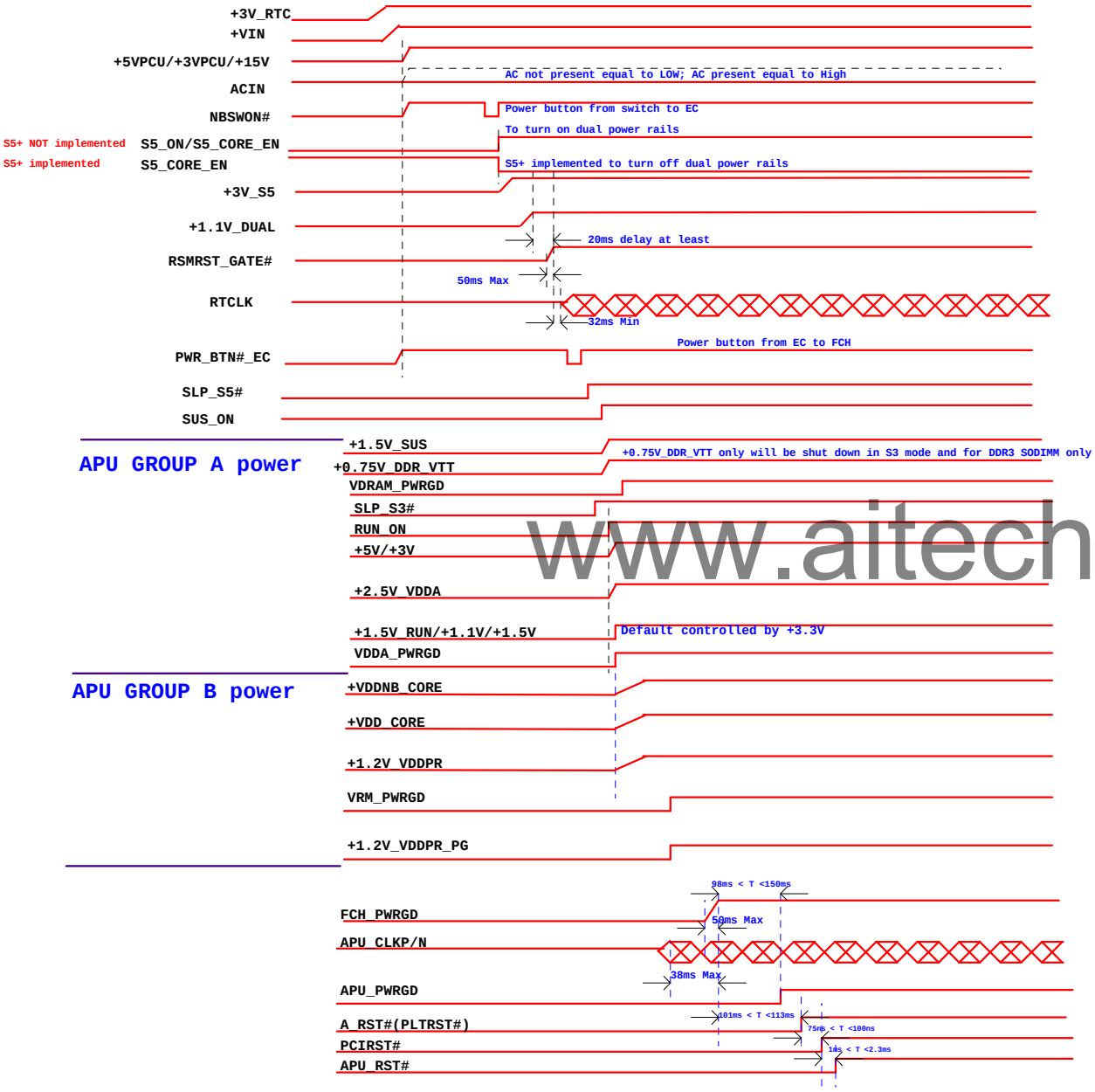


Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	System Block Diagram	1C

Date: Tuesday, April 19, 2011 Sheet 1 of 53

BLF/BLFD Power On Sequence: S5 > S0



APU Power on sequence required:

Llano APU:
1.Group A (+1.5V_SUS, +2.5V_VDDA) ramp before Group B (+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M2/M3:
1.+3V_S5 ramp before +1.1V_DUAL
2.+3V ramp before +1.1V
3.+3V_RTC must ramp at least 5 secs before the +3V_S5

Seymour XT S3 package Power-on sequence

All power rails reach nominal within 20ms

1 => +3V_GPU
2 => +VGPU_CORE/+1V_GPU
3 => +VGPU_CORE PWRGD to enable +1.5V_GPU
4.=> +1V_GPU PWRGD to enable +1.8V_GPU

NOTE

1.+3V to turn on +3V_GPU

2.+3V_GPU ready to enable +VGPU_CORE/+1V_GPU
(+1V_GPU will ramp up before +VGPU_CORE)

3.+VGPU_CORE PWRGD to enable +1.5V_GPU

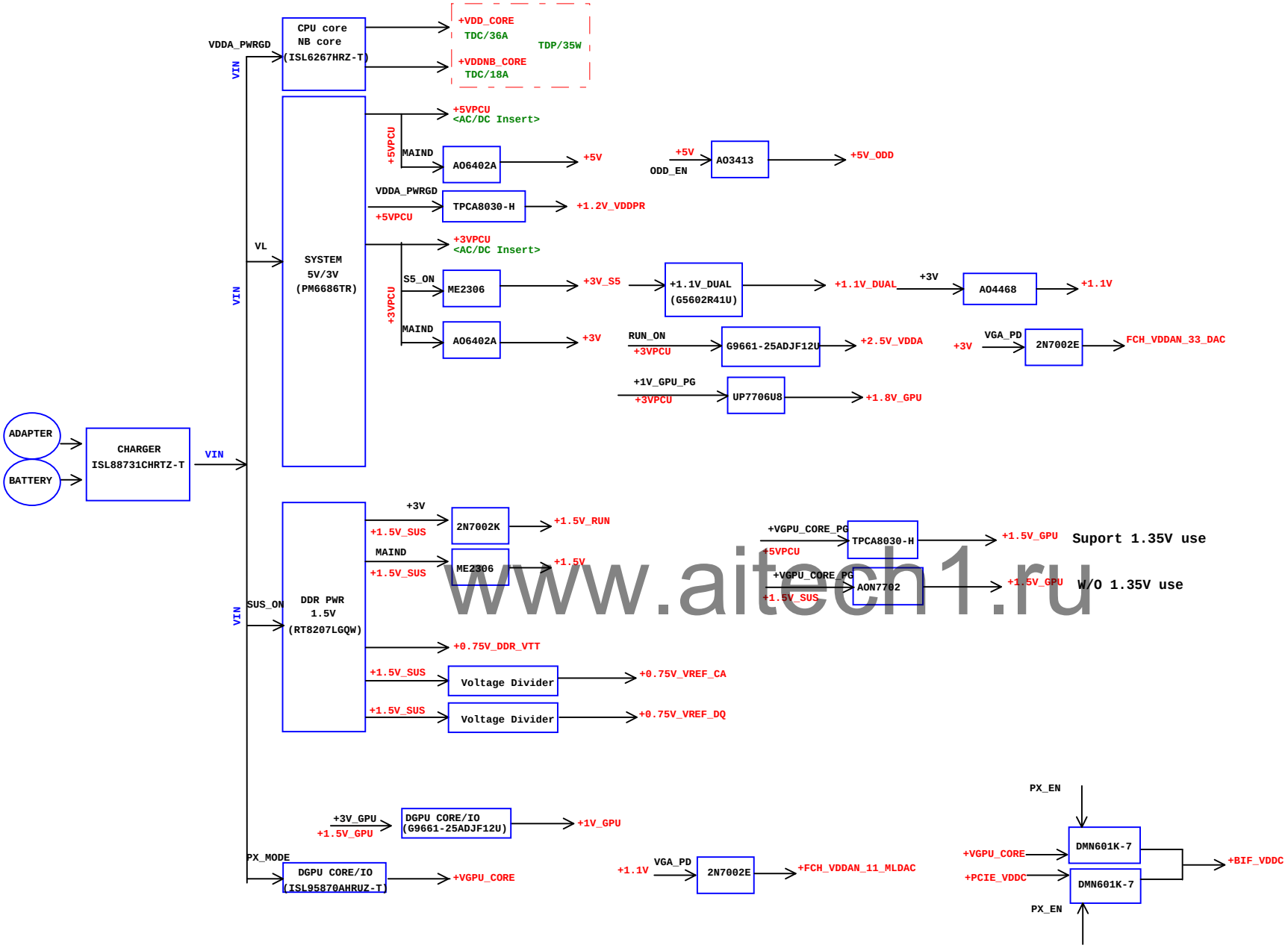
3.+1V_GPU PWRGD to enable +1.8V_GPU

TRAVIS_L ANX3110 power on sequecne

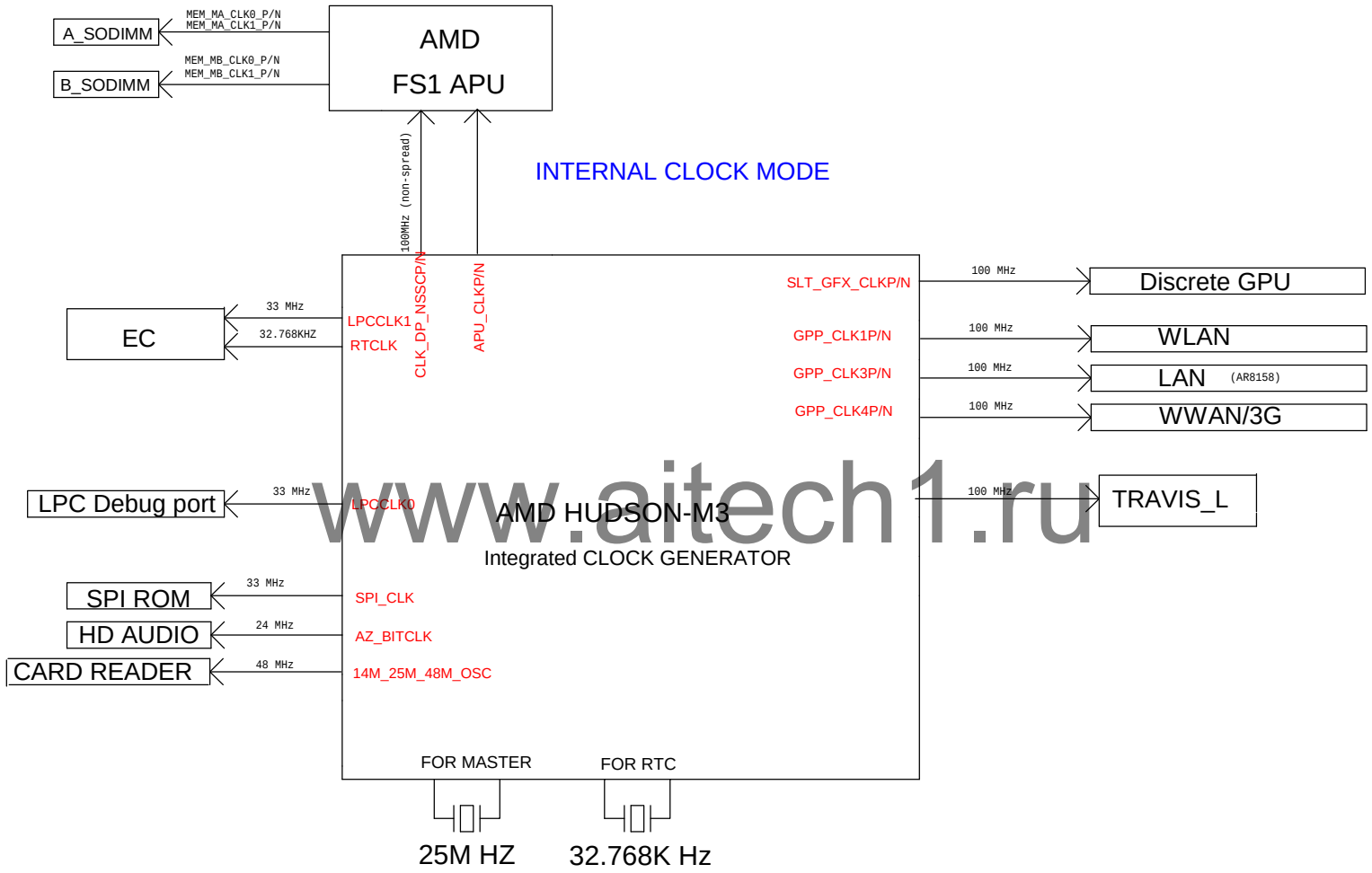
1.+3V must lead +1.2V_TRAVIS

2.+1.2V_TRAVIS must lead TRAVIS_RST#

NOTE: FCH must output PCIE_RST#_TRAVIS or APU_PCIE_RST# after +1.2V_TRAVIS ready



Quanta Computer Inc.
PROJECT : BLF_BLFD
Power Tree
Tuesday, April 19, 2011

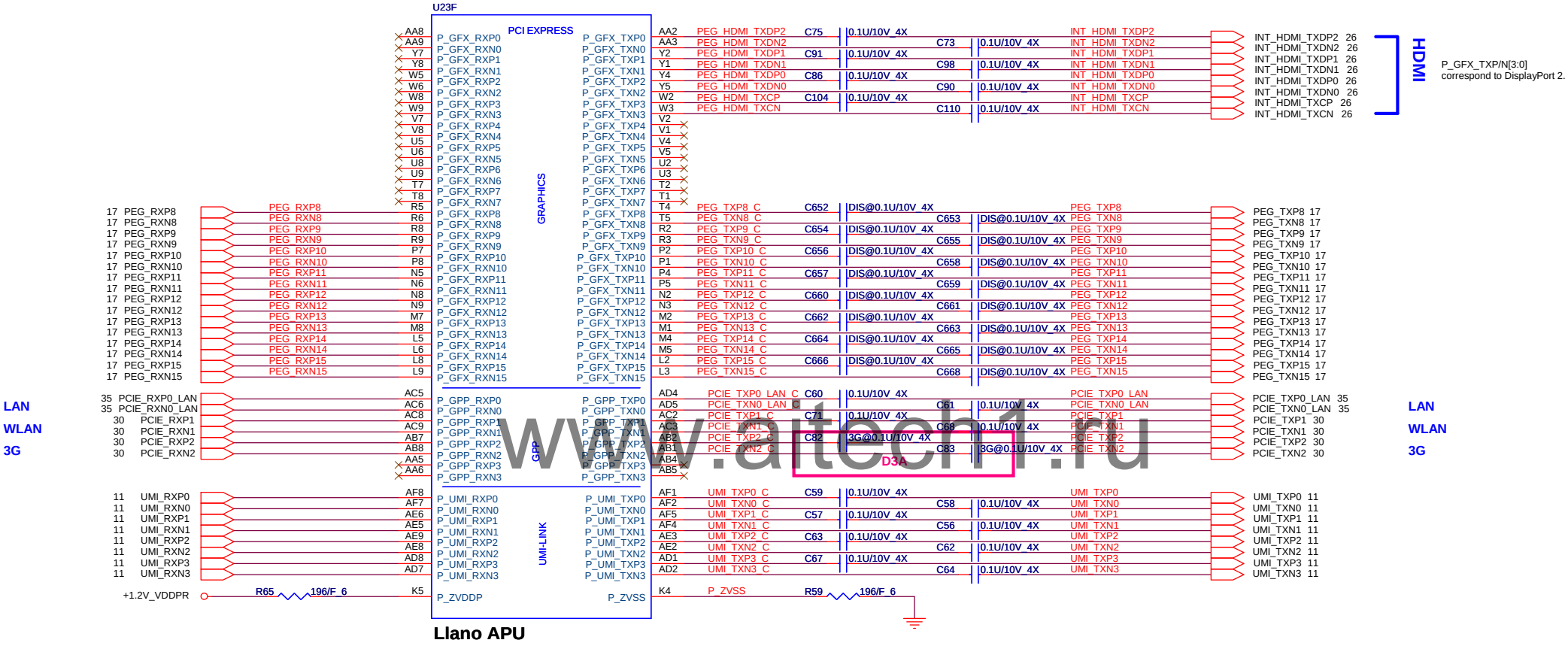


Quanta Computer Inc.

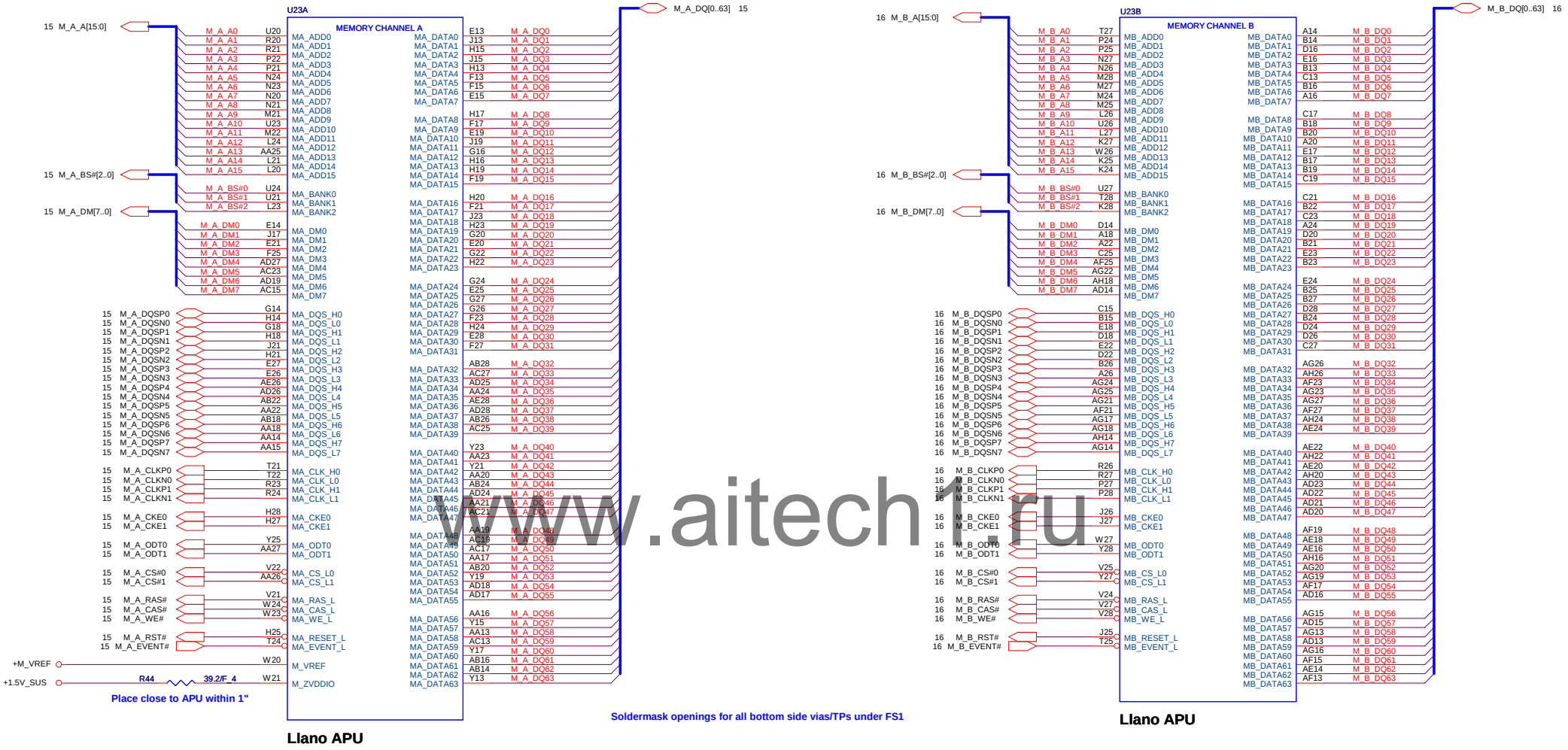
PROJECT : BLF_BLFD

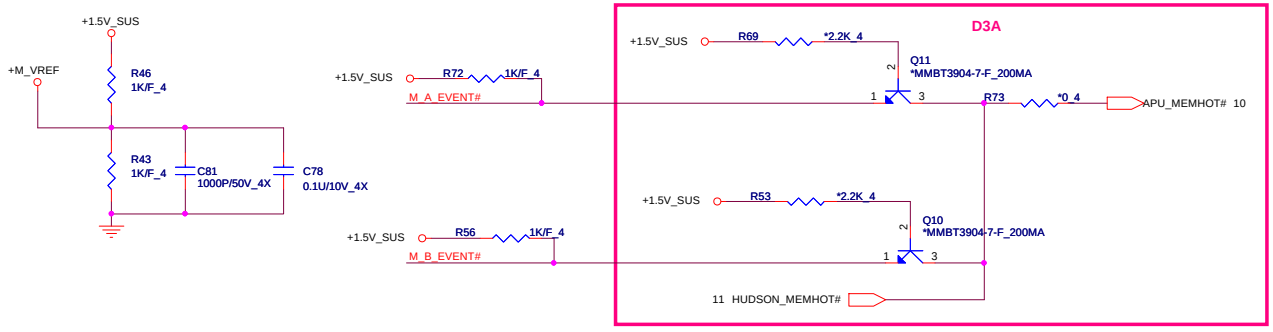
Size	Document Number	Rev
	Clock Distribution Diagram	1C

Date: Tuesday, April 19, 2011 Sheet 4 of 53



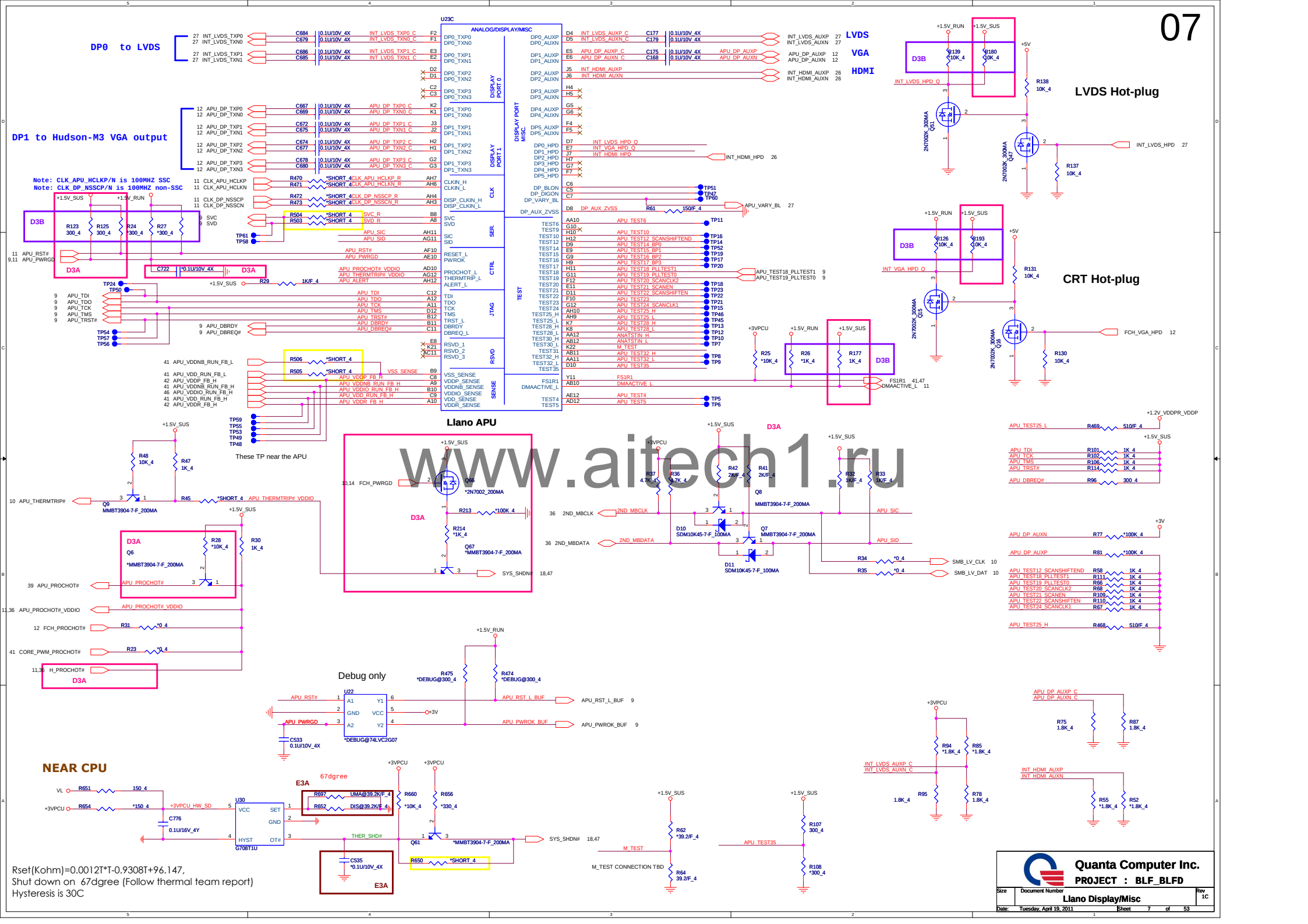
Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: Llano PCIE/UMI/GPP	Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 5 of 53	





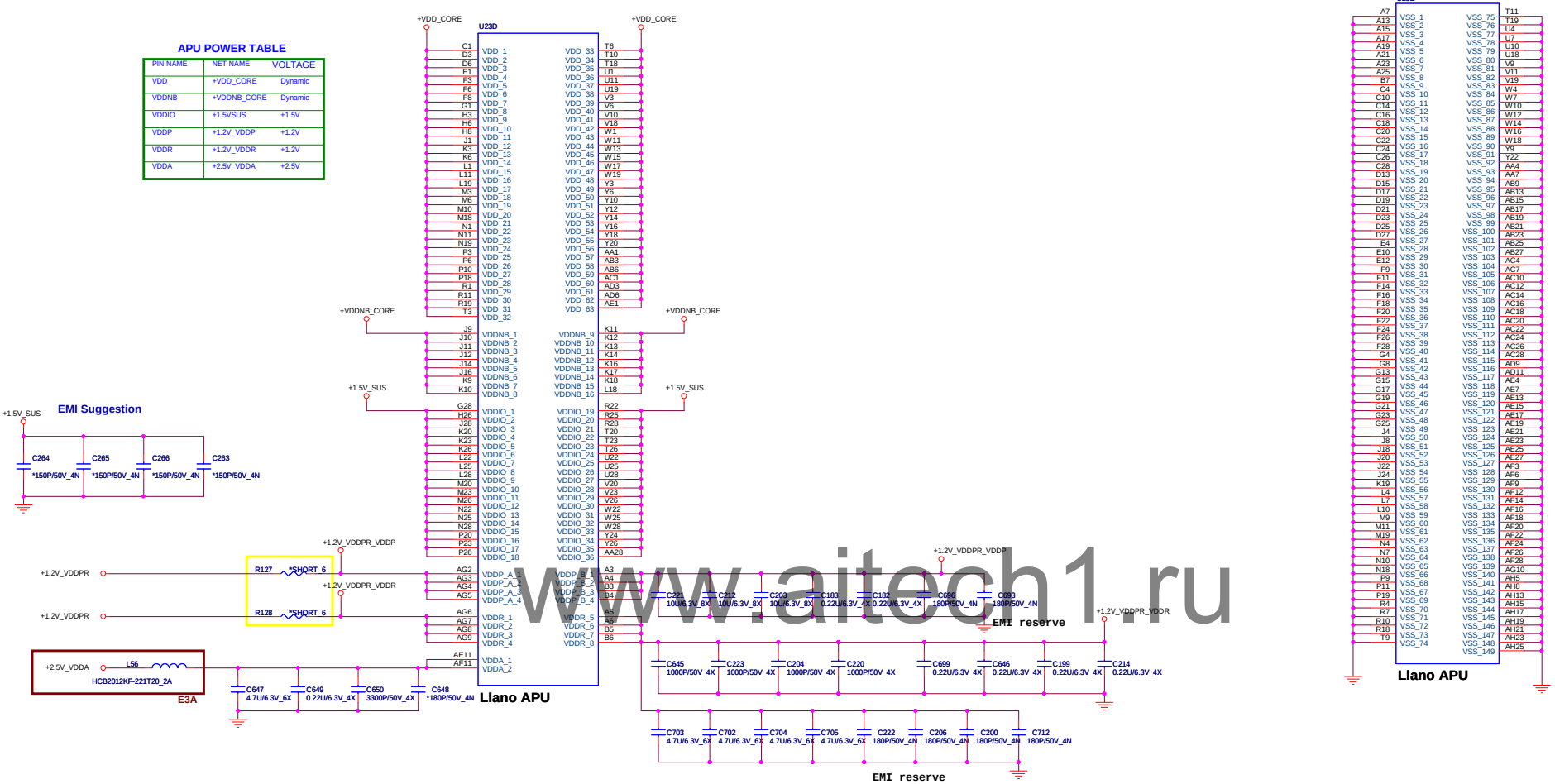
Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Llano DDR3 MEM I/F	1C
Date: Tuesday, April 19, 2011	Sheet 6 of 53	

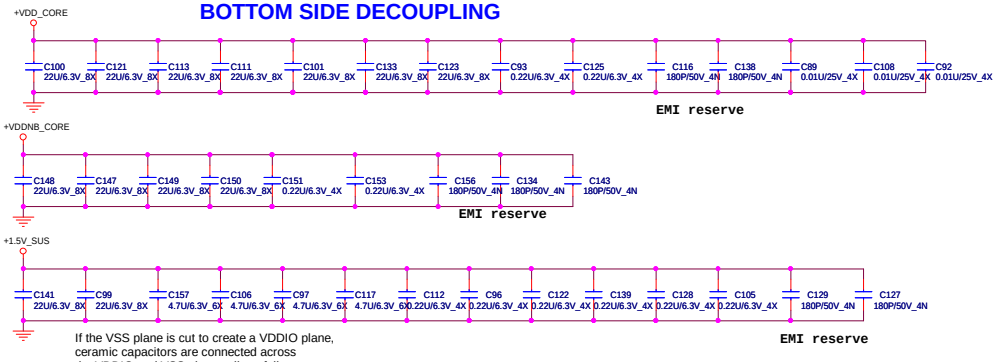


APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	Dynamic
VDDNB	+VDDNB_CORE	Dynamic
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



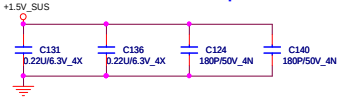
BOTTOM SIDE DECOUPLING



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

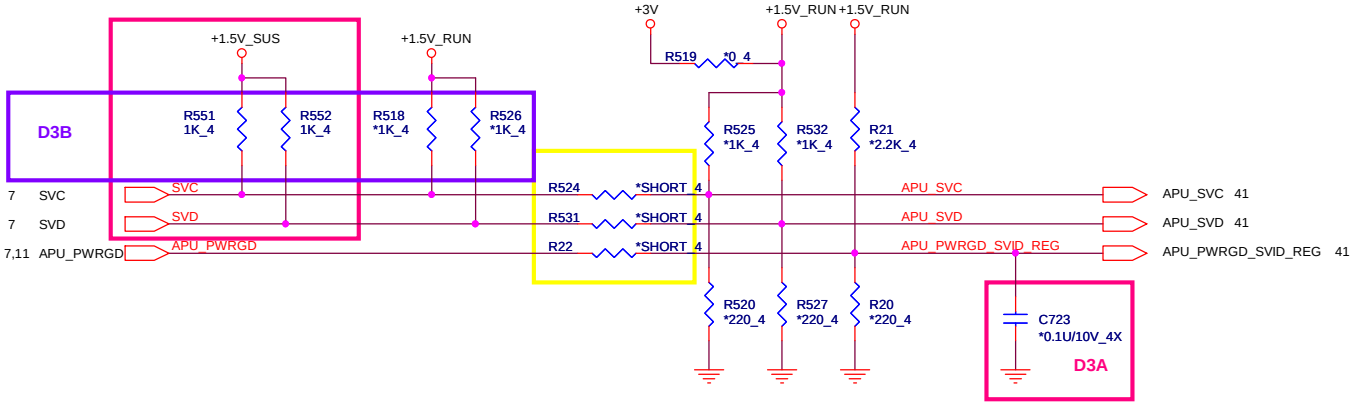
DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split



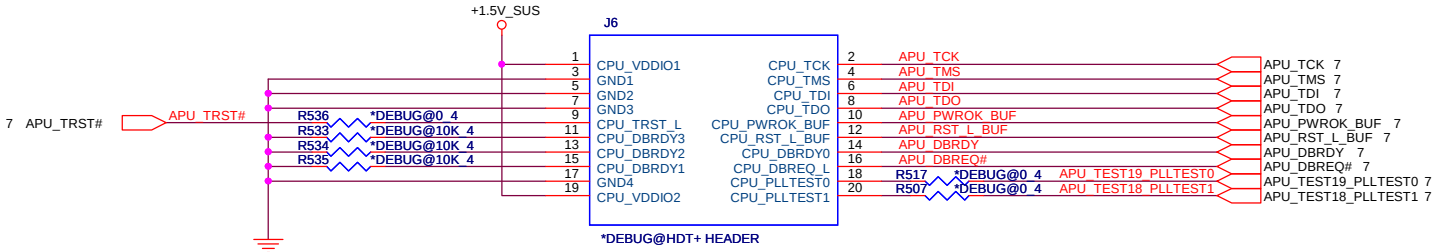
Quanta Computer Inc.	PROJECT : BLF_BLFD	
Size	Document Number: Llano POWER/GND	Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 8 of 53	

VID Override Circuit

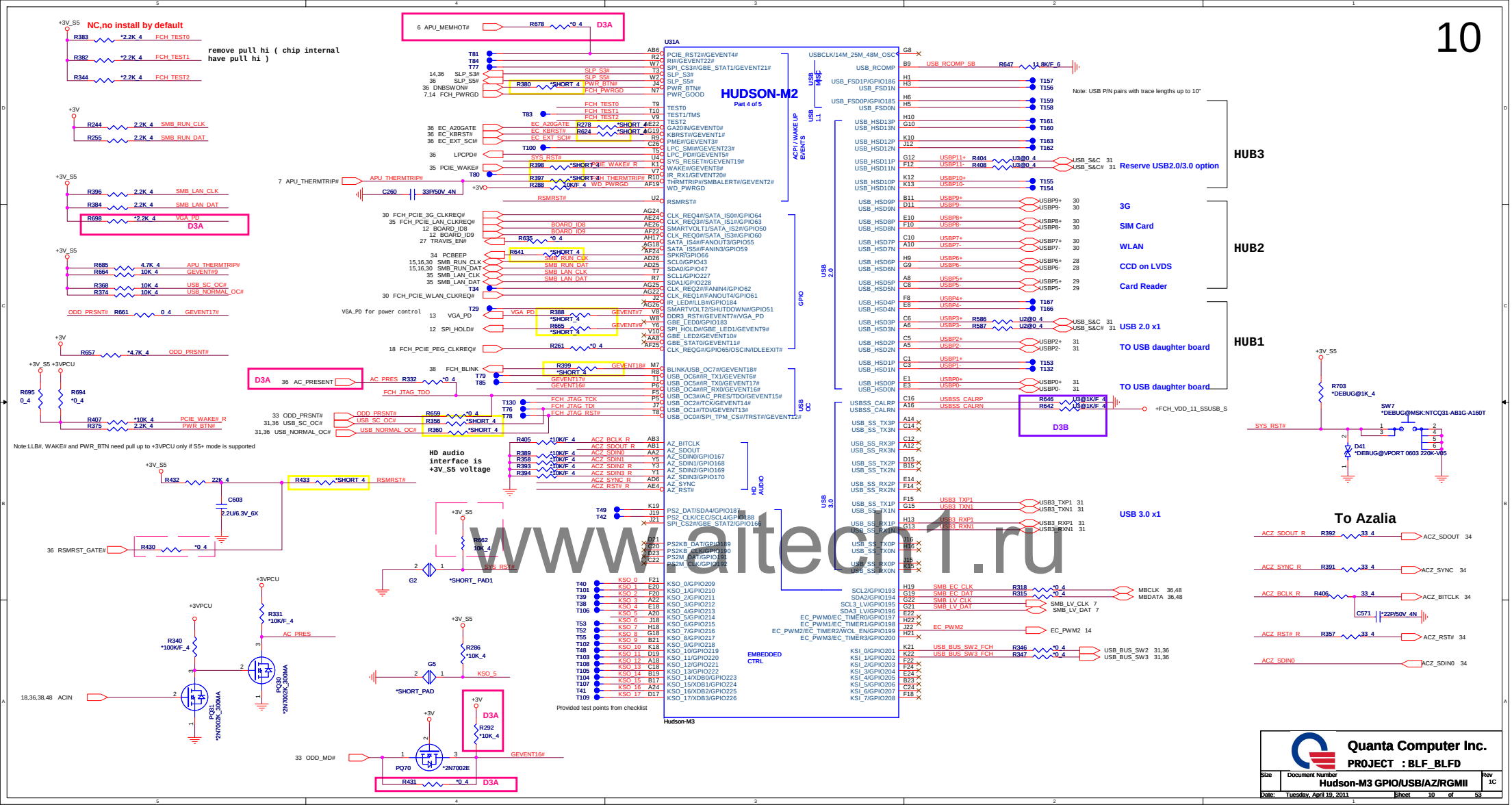


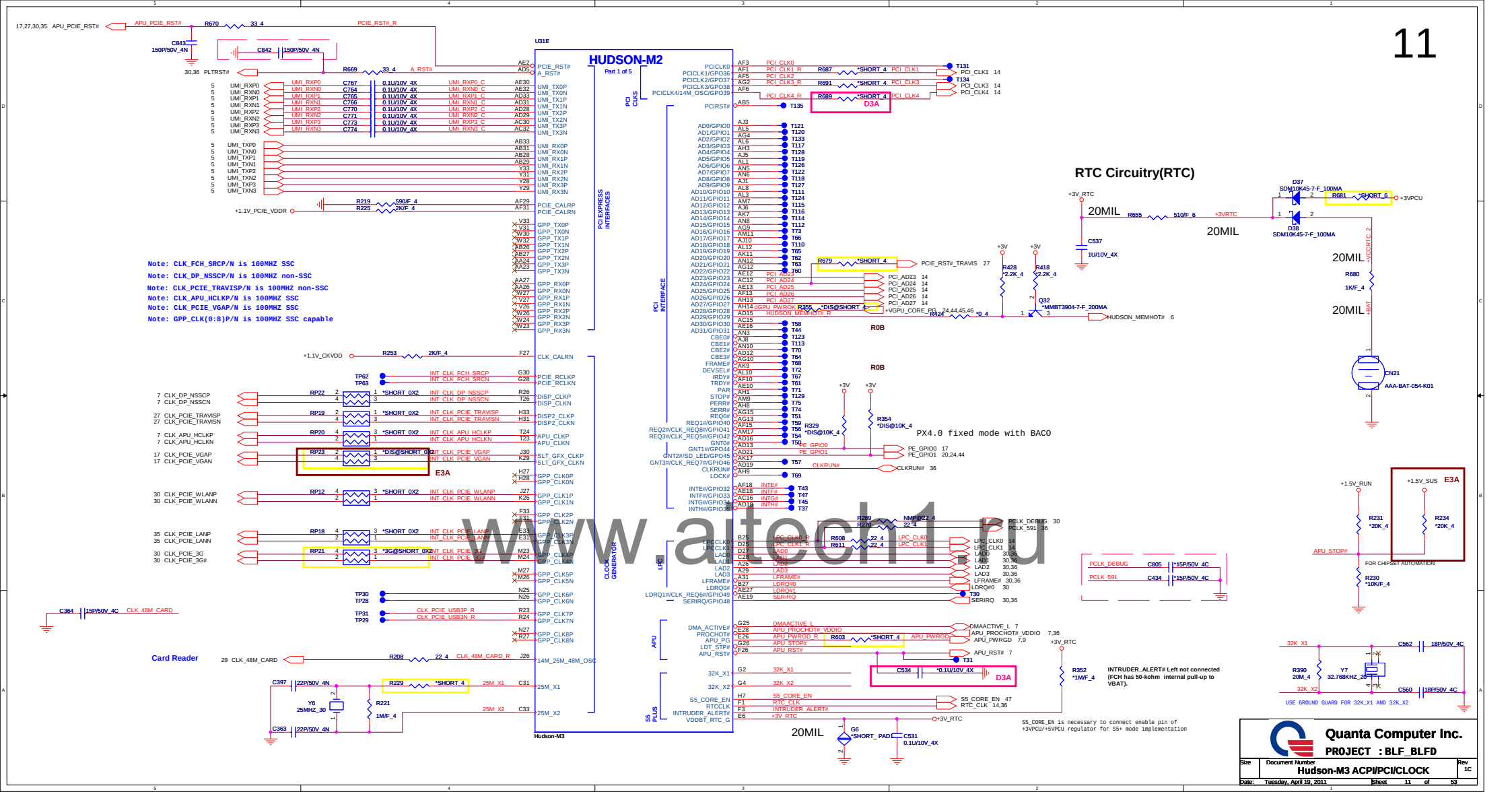
HDT+ Connector

Debug only



Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: Llano DEBUG&OTHER	Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 9 of 53	

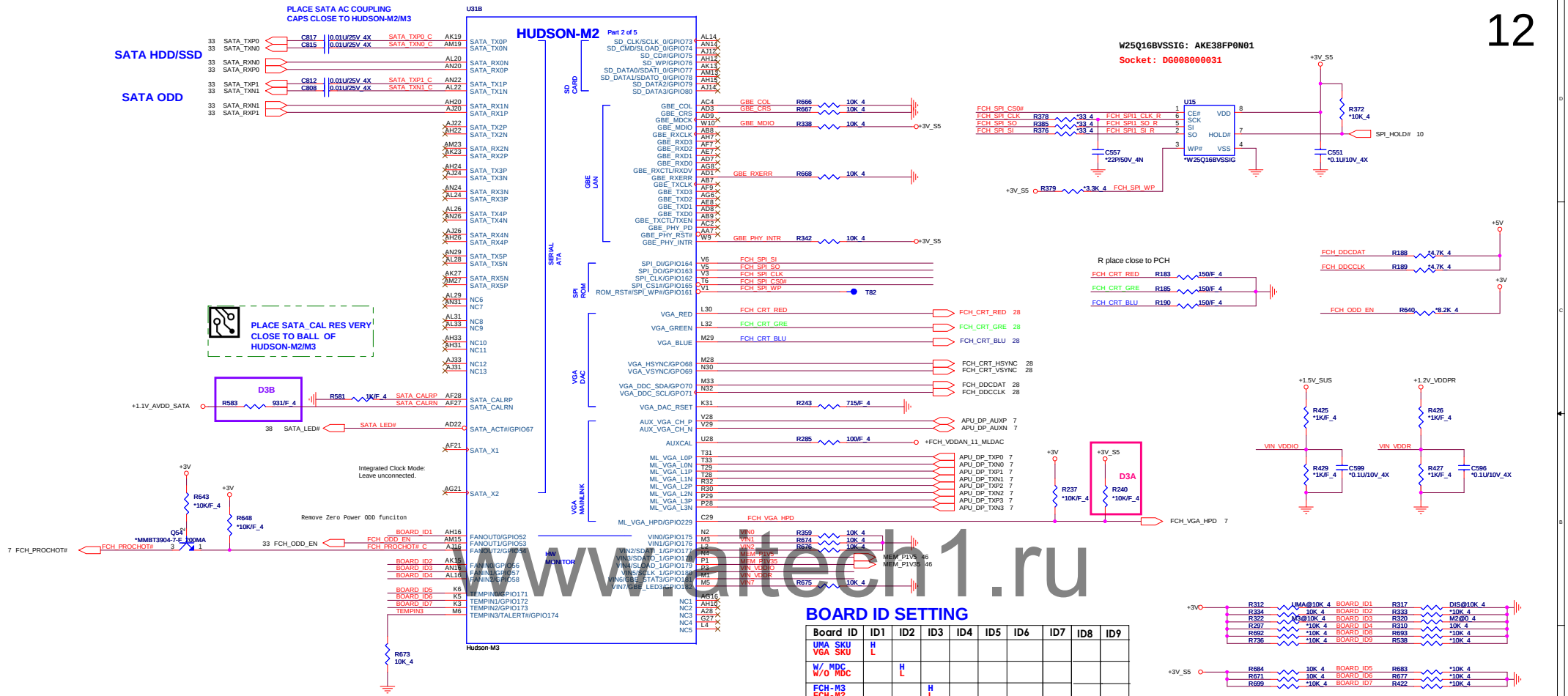




Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Hudson-M3 ACPI/PCI/CLOCK	1C

Date: Tuesday, April 19, 2011 Sheet 11 of 53



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDQ--3.3V I/O power 102mA

VDD-- S/B CORE power

CKVDD_1.1V-- Internal clock Generator I/O power

PCIE_VDDR--PCIE I/O power

AVDD_SATA--SATA phy power

S5_3.3--3.3v standby power

S5_1.1V--1.1V standby power

S5 plus mode

HUDSON-M2 Part 3 of 3 (U31C)

HUDSON-M2 Part 5 of 5 (U31D)

Hudson-M3

Hudson-M3 POWER/GND

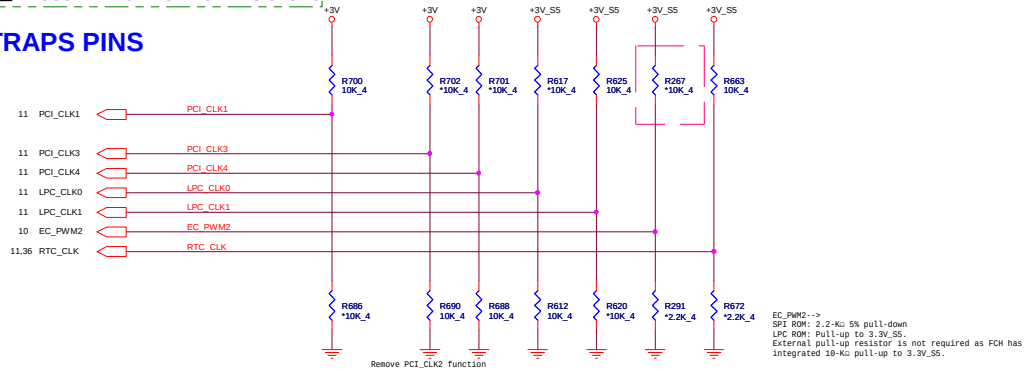
32 mA Max

233 mA Max

Quanta Computer Inc.
PROJECT : BLF_BLFD
Size | Document Number: Hudson-M3 POWER/GND | Rev 1C
Date: Tuesday, April 19, 2011 | Sheet 13 of 53

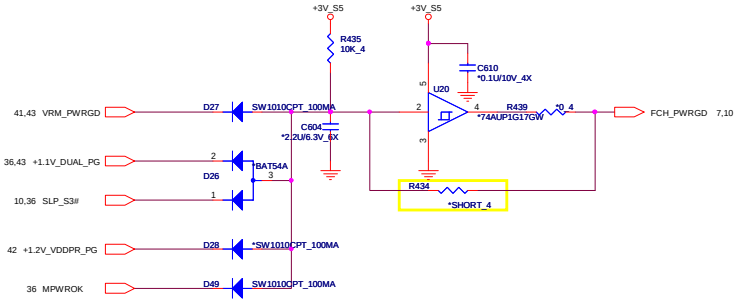
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS



REQUIRED STRAPS

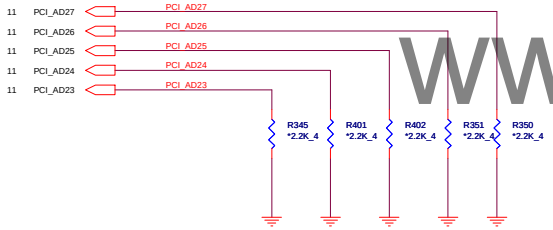
	--------	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED



FCH PWRGD CKT

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



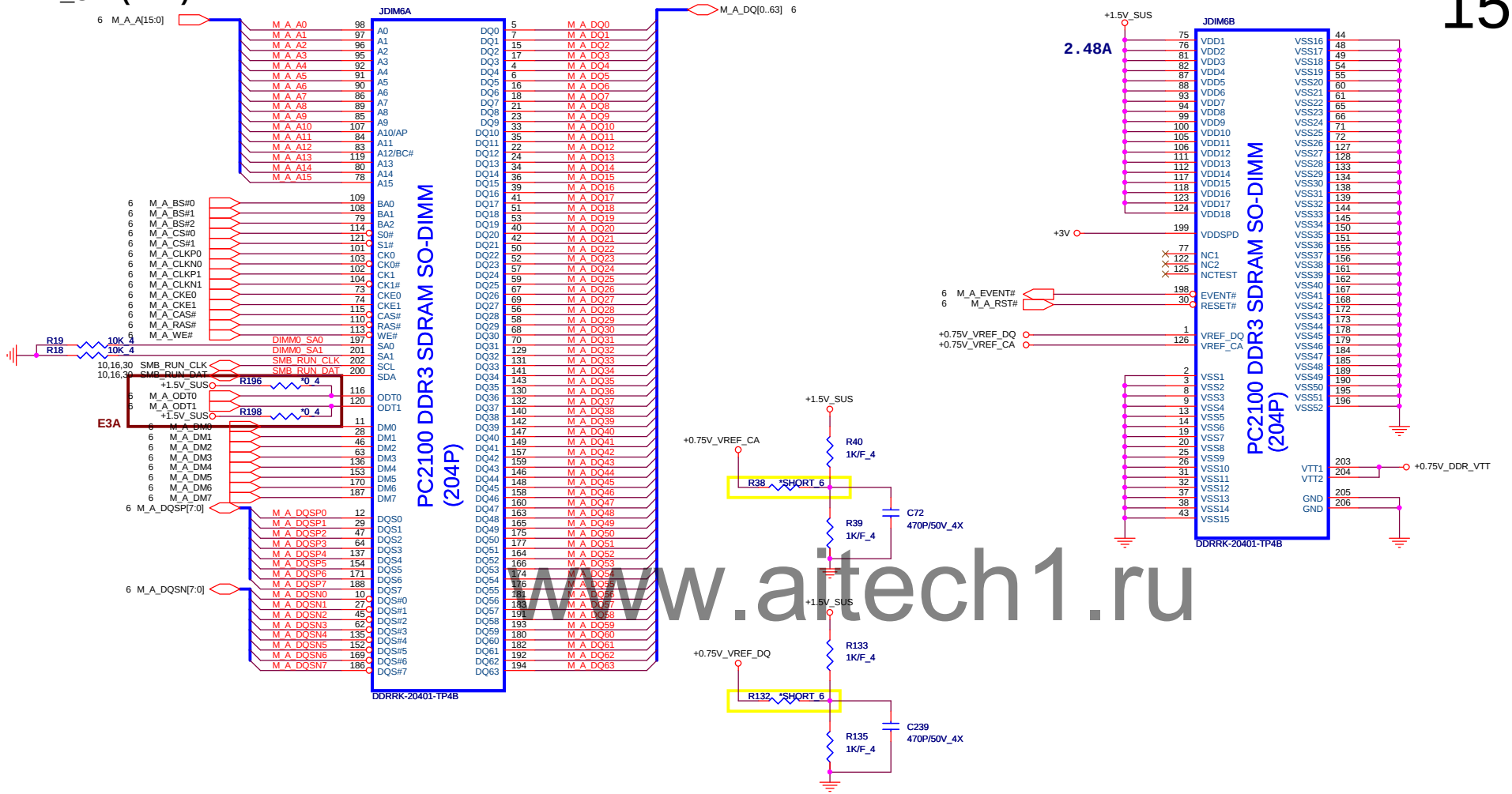
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Quanta Computer Inc.
PROJECT : BLF_BLFD

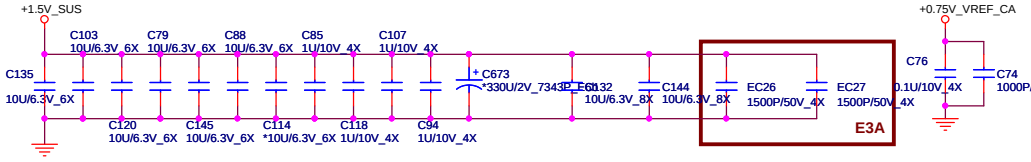
Size	Document Number	Rev
	Hudson-M3 STRAP/PWRGD	1C

Date: Tuesday, April 19, 2011 Sheet 14 of 53

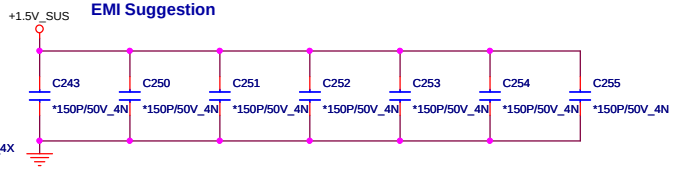
DDR_STD(DDR)

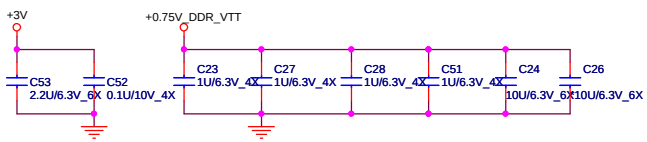


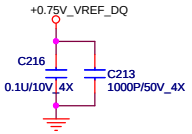
Place these Caps near So-Dimm0.



EMI Suggestion

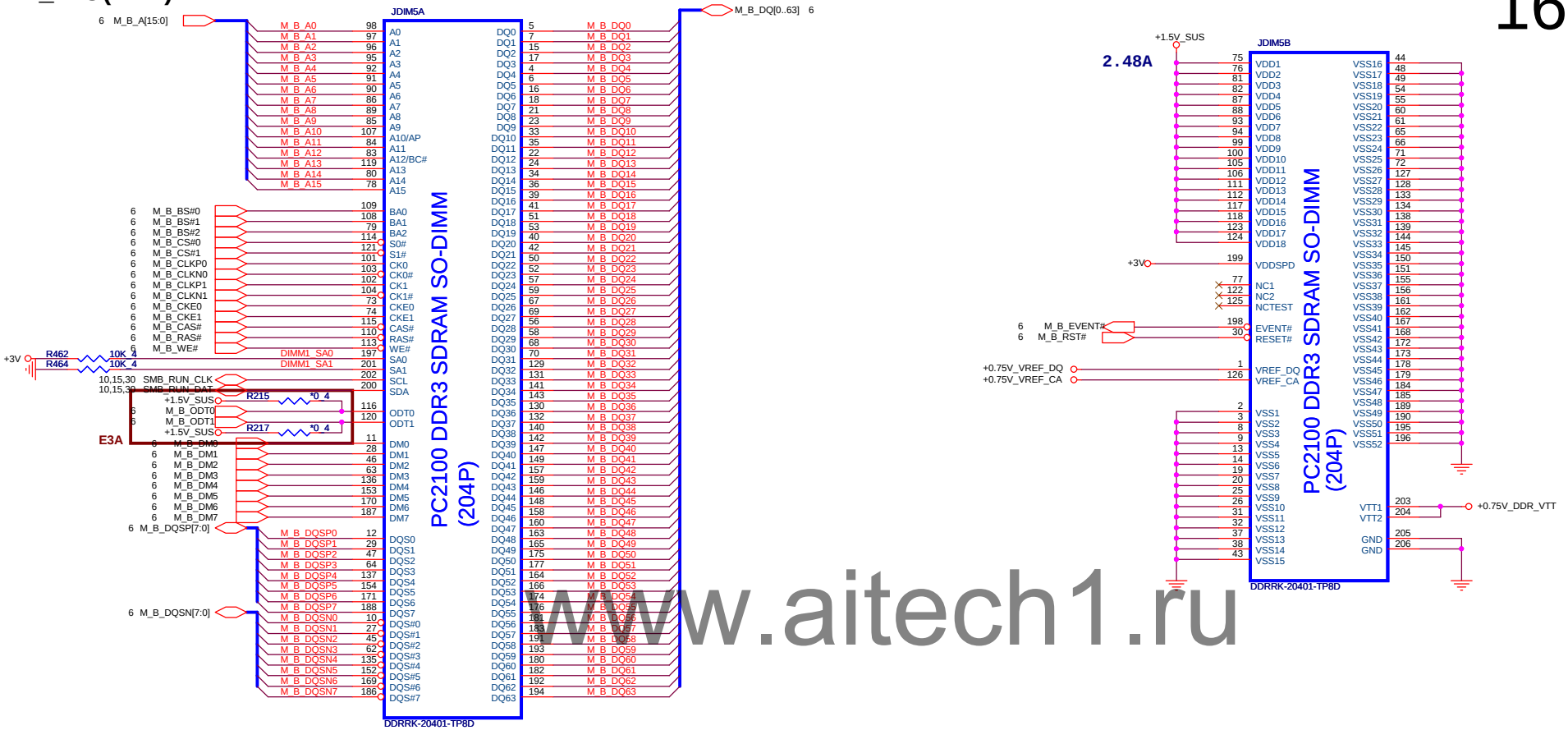


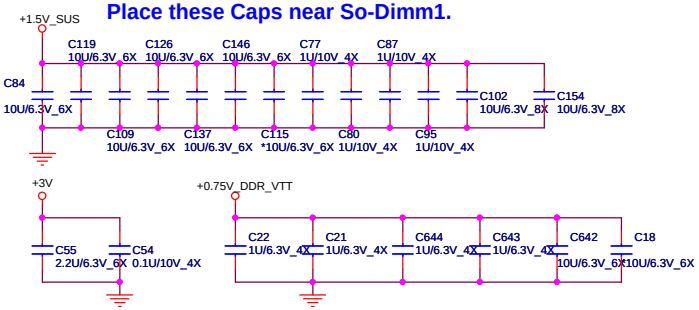


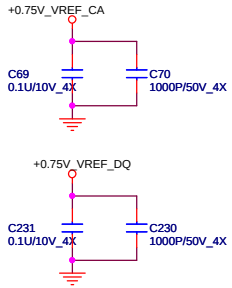


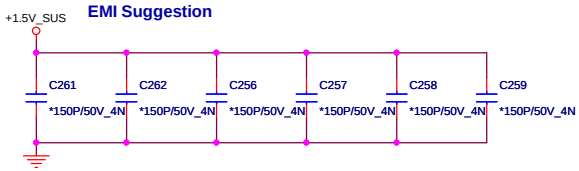
Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: DDRIII SO-DIMM-0	Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 15 of 53	

DDR_RVS(DDR)









Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1C

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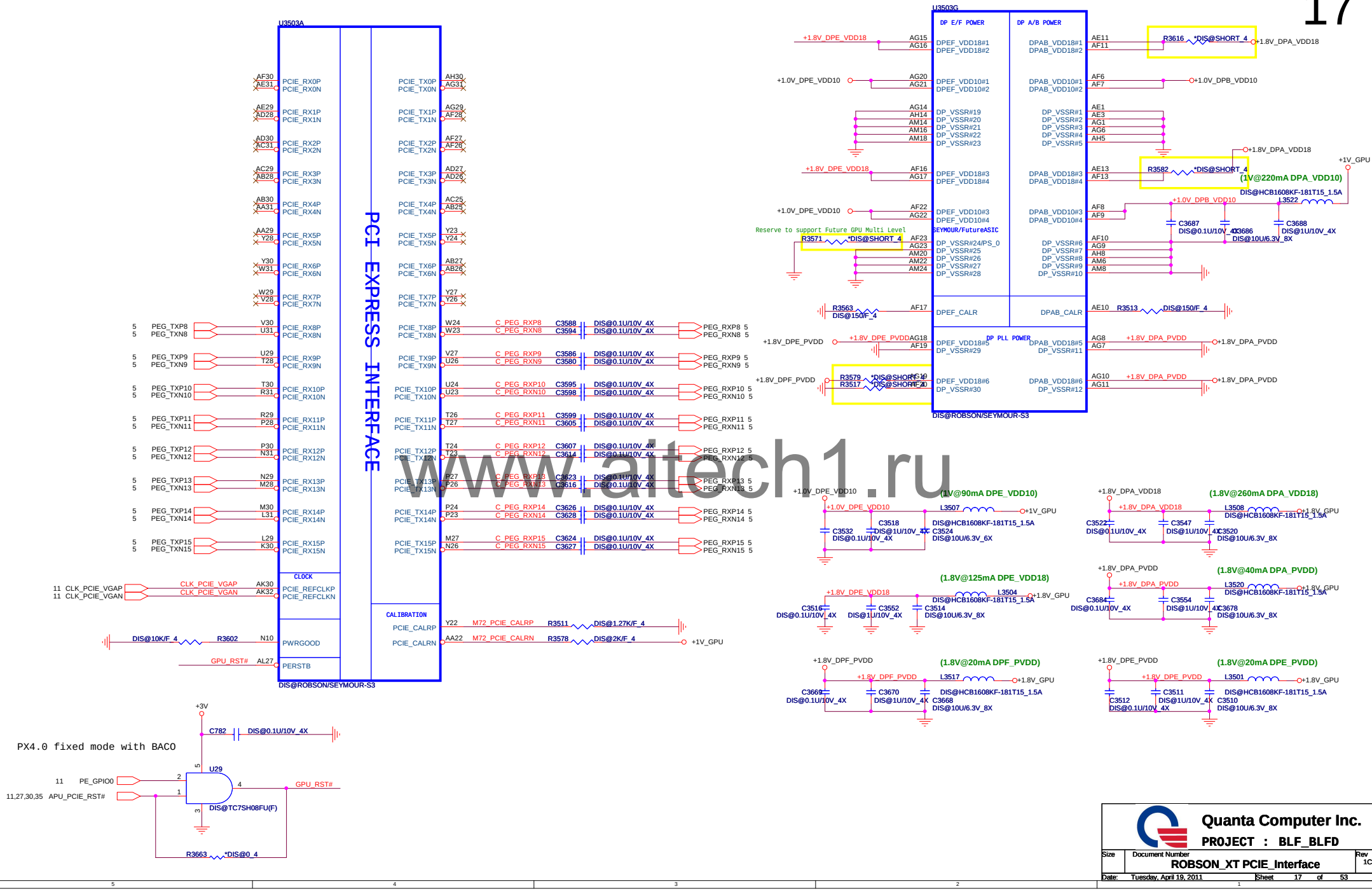
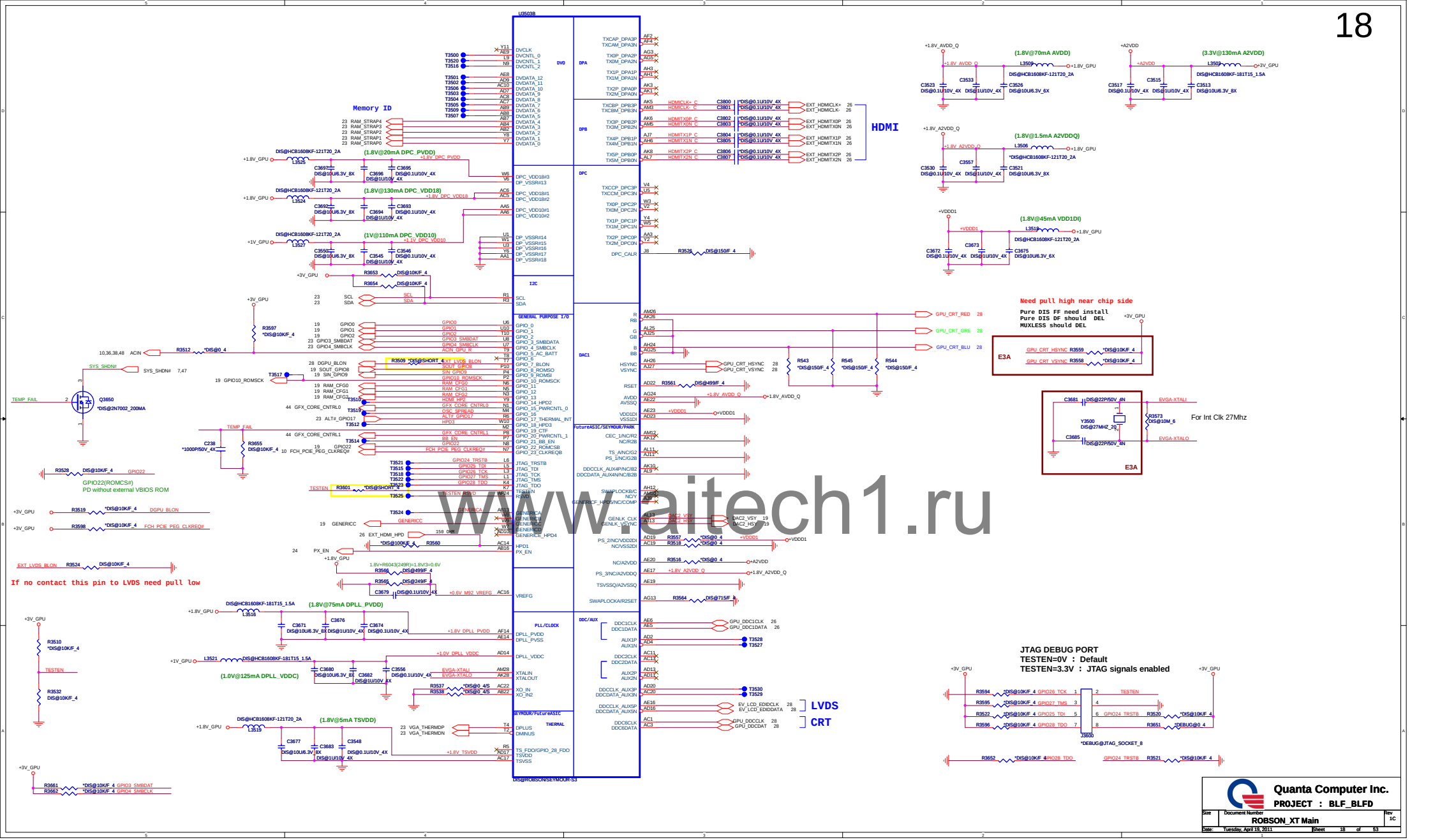
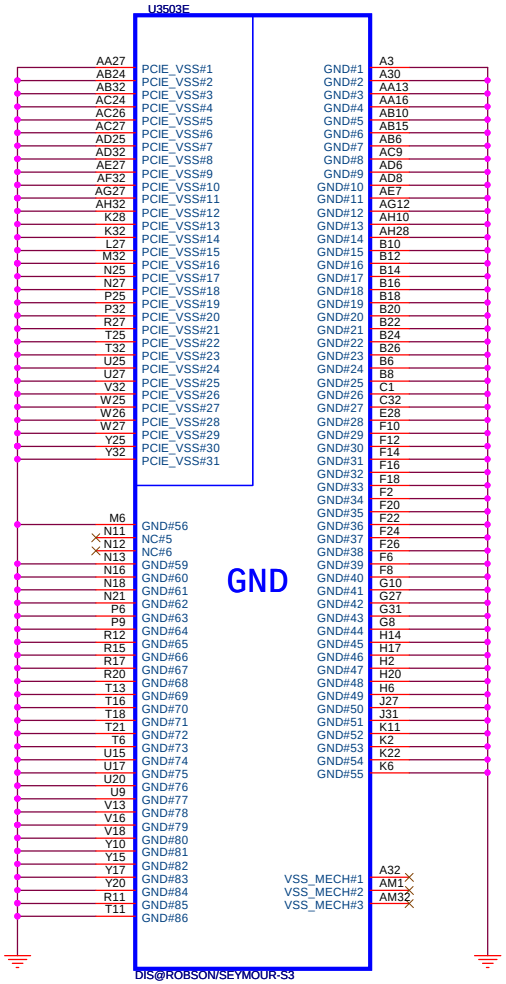
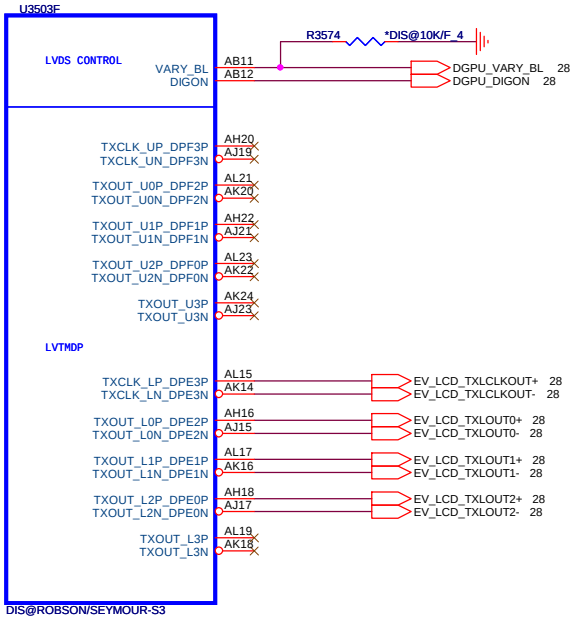


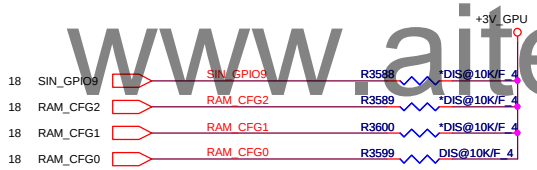
Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: ROBSON_XT PCIE_Interface	Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 17 of 53	



Reserve only for MUXLESS







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

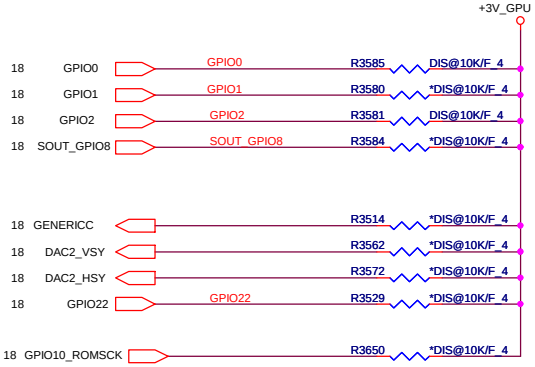
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

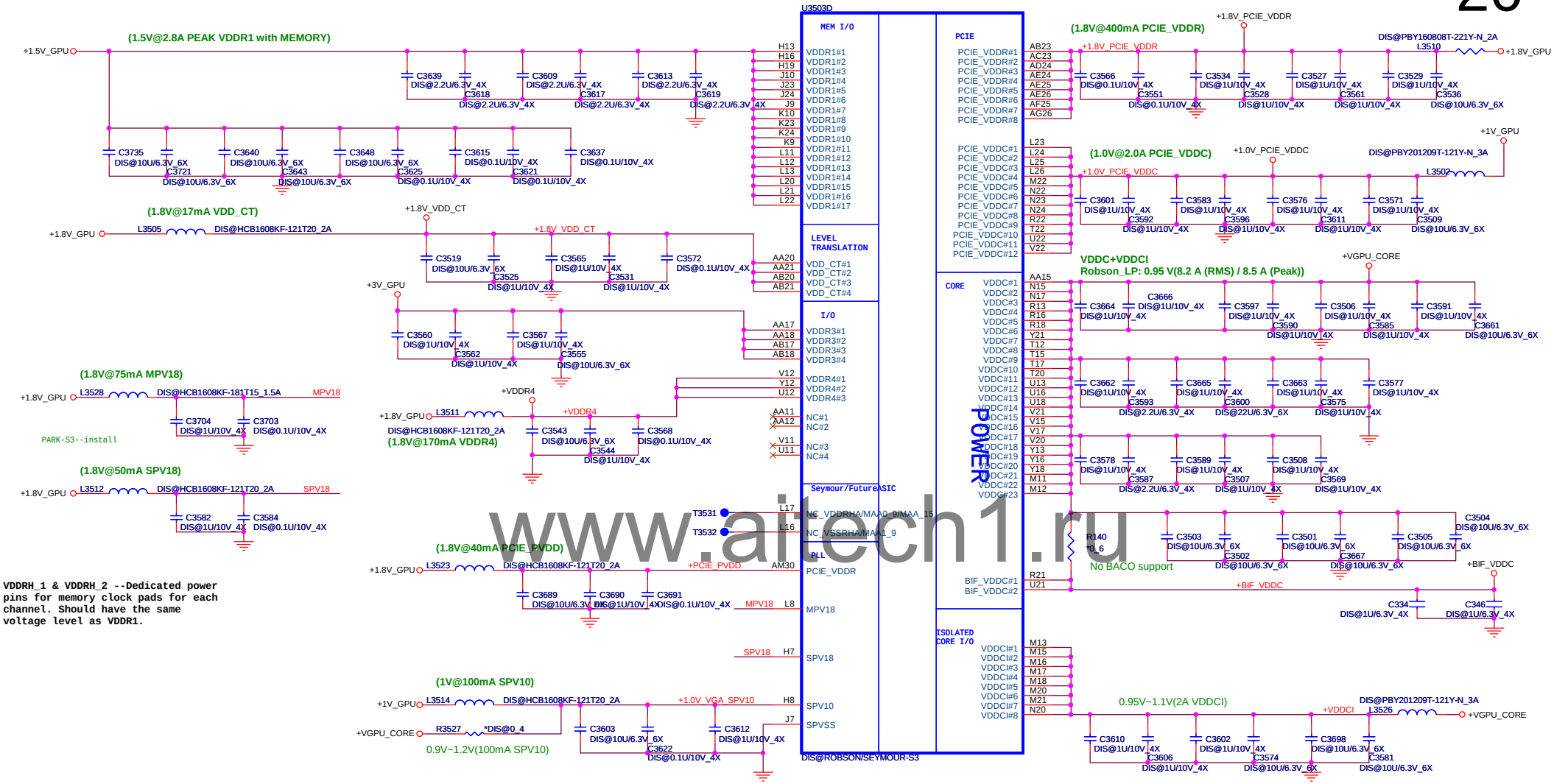
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	ROBSON_XT GND / LVDS/ Straps	1C
Date: Tuesday, April 19, 2011	Sheet 19 of 53	

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

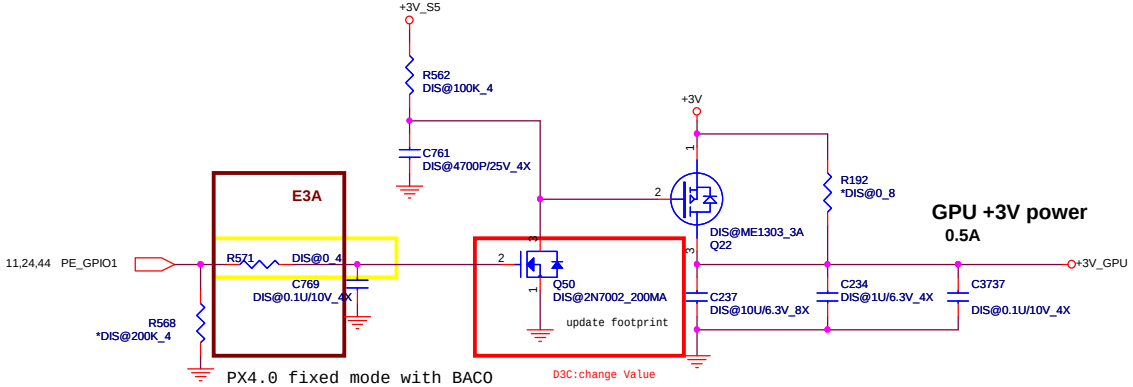


VDDRH_1 & VDDRH_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.

VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

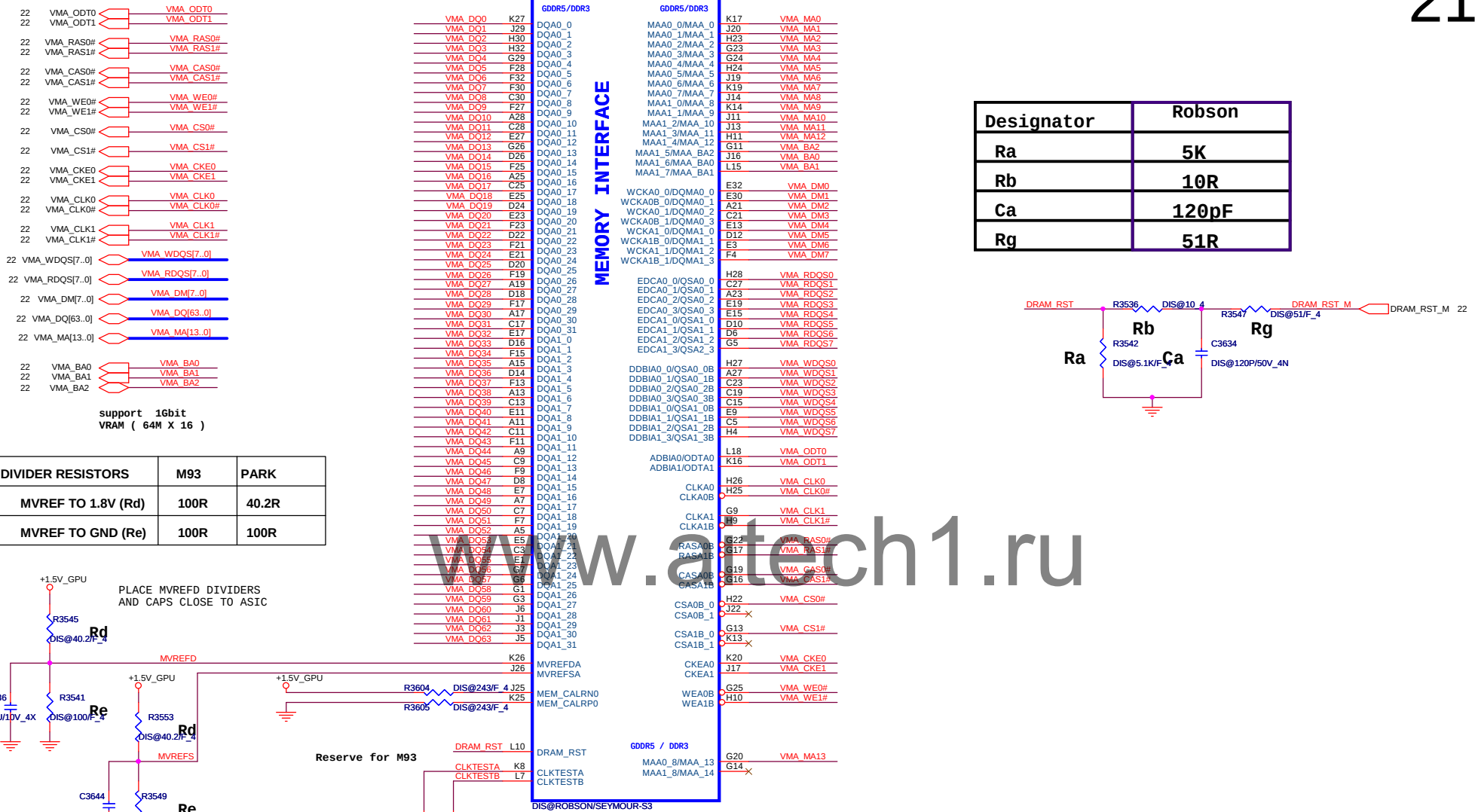
PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%



Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	ROBSON_Power_and_NC	1C
Date: Tuesday, April 19, 2011	Sheet 20 of 53	



DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

Designator	Robson
Ra	5K
Rb	10R
Ca	120pF
Rg	51R

Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	ROBSON/MEM_Interface	1C

Date: Tuesday, April 19, 2011 Sheet 21 of 53

512MB DDR3

21 VMA_MA[13..0]
21 VMA_DM[7..0]
VMA_MA[13..0]
21 VMA_DQ[63..0]
21 VMA_WDQS[7..0]
21 VMA_RDQS[7..0]

U3501 — U3504 — U3500 — U3505

100-BALL SDRAM DDR3
DIS@K4W1G1646G-BC11

Should be 240 Ohms +-1%
R3552 DIS@243/F_4
R3609 DIS@243/F_4
R3546 DIS@243/F_4
R3606 DIS@243/F_4

+1.5V_GPU

R3613 DIS@4.99K/F_4
R3533 DIS@4.99K/F_4
R3611 DIS@4.99K/F_4
R3534 DIS@4.99K/F_4
R3556 DIS@4.99K/F_4
R3550 DIS@4.99K/F_4
R3608 DIS@4.99K/F_4
R3603 DIS@4.99K/F_4

VREFC_VMA1 VREFD_VMA1 VREFC_VMA2 VREFD_VMA2 VREFC_VMA3 VREFD_VMA3 VREFC_VMA4 VREFD_VMA4

R3612 DIS@4.99K/F_4 C3723 DIS@0.1U/10V_4X
R3535 DIS@4.99K/F_4 C3638 DIS@0.1U/10V_4X
R3614 DIS@4.99K/F_4 C3729 DIS@0.1U/10V_4X
R3539 DIS@4.99K/F_4 C3715 DIS@0.1U/10V_4X
R3555 DIS@4.99K/F_4 C3649 DIS@0.1U/10V_4X
R3554 DIS@4.99K/F_4 C3645 DIS@0.1U/10V_4X
R3610 DIS@4.99K/F_4 C3719 DIS@0.1U/10V_4X
R3607 DIS@4.99K/F_4 C3714 DIS@0.1U/10V_4X

VMA_CLK0 R3543 DIS@56.2/F_4 C3642 VMA_CLK0_COMM DIS@0.01U/25V_4X R3548 DIS@56.2/F_4 VMA_CLK0#
VMA_CLK1 R3540 DIS@56.2/F_4 C3635 VMA_CLK1_COMM DIS@0.01U/25V_4X R3544 DIS@56.2/F_4 VMA_CLK1#

+1.5V_GPU decoupling: C3632 C3655 C3641 C3630 C3633 C3646 C3631 C3732 DIS@1U/6.3V_4X
C3709 C3707 C3730 C3629 C3733 C3724 C3706 C3705 C3736 C3726 C3652 C3727 C3734 C3650 C3654 C3731 C3712 C3708 C3717 C3718 C3720 C3647 C3651 C3710 DIS@1U/6.3V_4X
C3728 C3658 C3657 C3711 C3660 C3713 C3725 C3656 C3653 C3722 C3716 C3659 DIS@10U/6.3V_6X

	QCI PN
SAMSUNG	AKD5MGWT500
HYNIX	AKD5MGWTW00

Quanta Computer Inc.
PROJECT : BLF_BLFD
Size | Document Number: Seymour S3 VRAM(DDR3 BGA96) | Rev 1C
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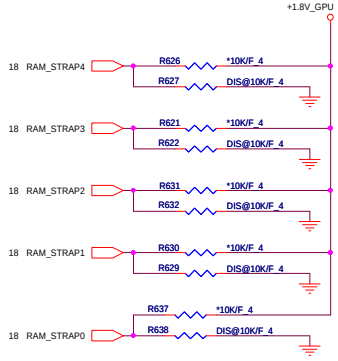
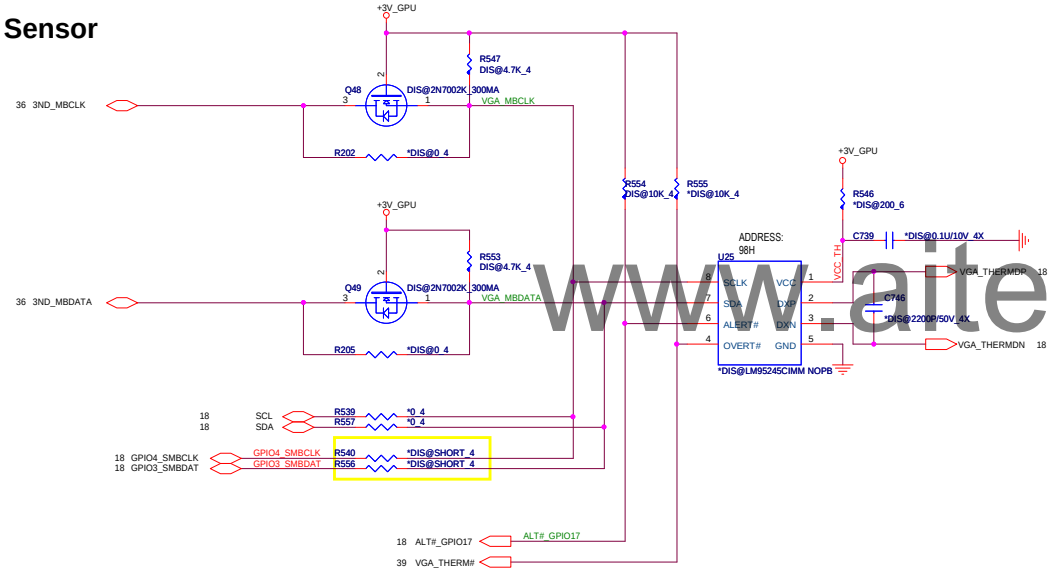
VRAM Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3	RAM_STRAP2	RAM_STRAP1	RAM_STRAP0	RAM_STRAP4	
				DVPDATA_3	DVPDATA_2	DVPDATA_1	DVPDATA_0	15"	14"
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW02 (64M*16-1Gb)	512MB	0	1	0	0	0	1
	H5TQ2G63BFR-11C	AKD5MGWTW00 (128M*16-2Gb)	1GB	0	0	0	0	0	1
Samsung	K4W1G1646G-BC11	AKD5EGGT500 (64M*16-1Gb)	512MB	0	1	0	1	0	1
	K4W2G1646C-HC11	AKD5MGWT500 (128M*16-2Gb)	1GB	0	0	0	1	0	1



Thermal Sensor



Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Blank	1C
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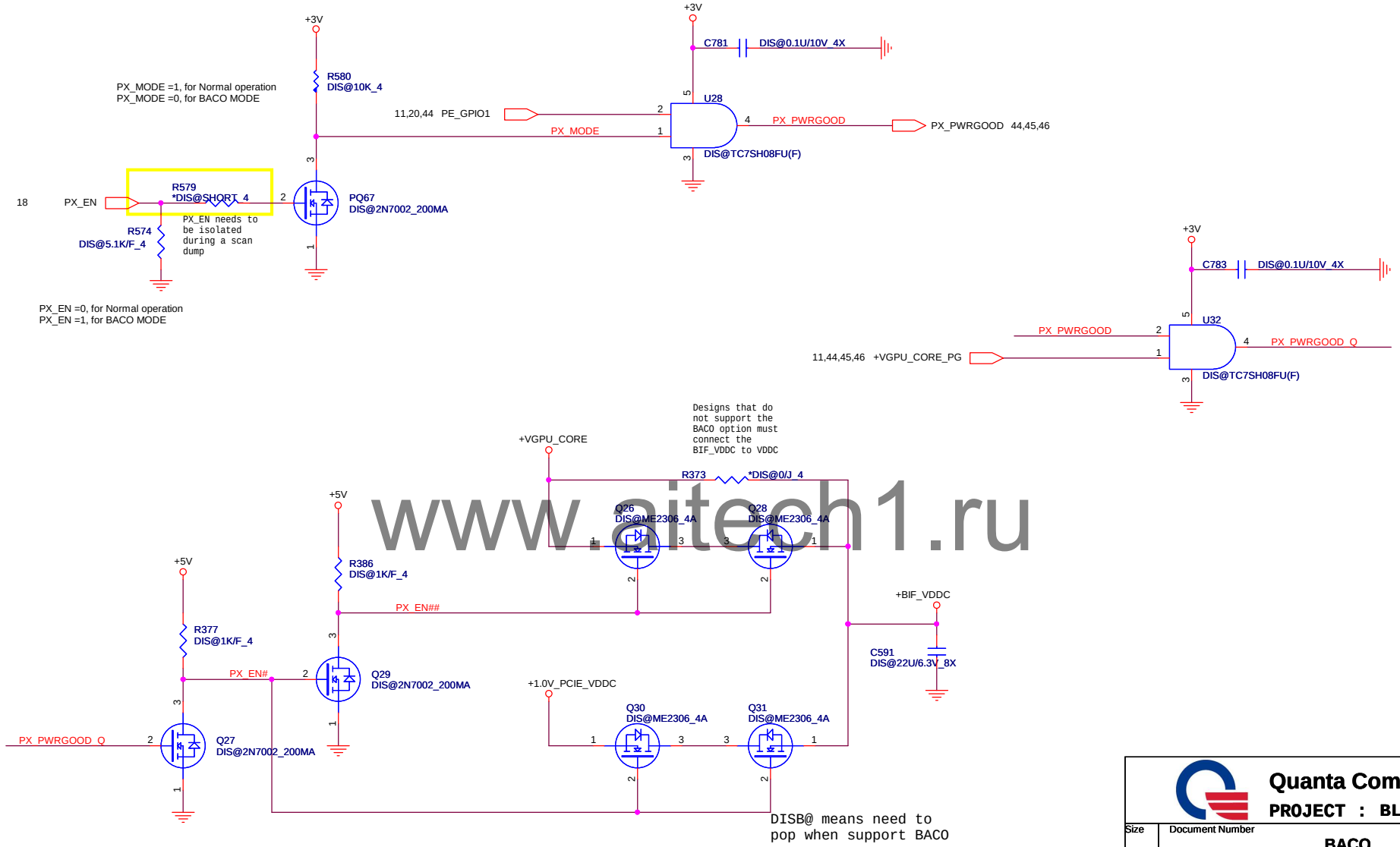

Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	BACO	1C

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Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: Blank	Rev: 1C
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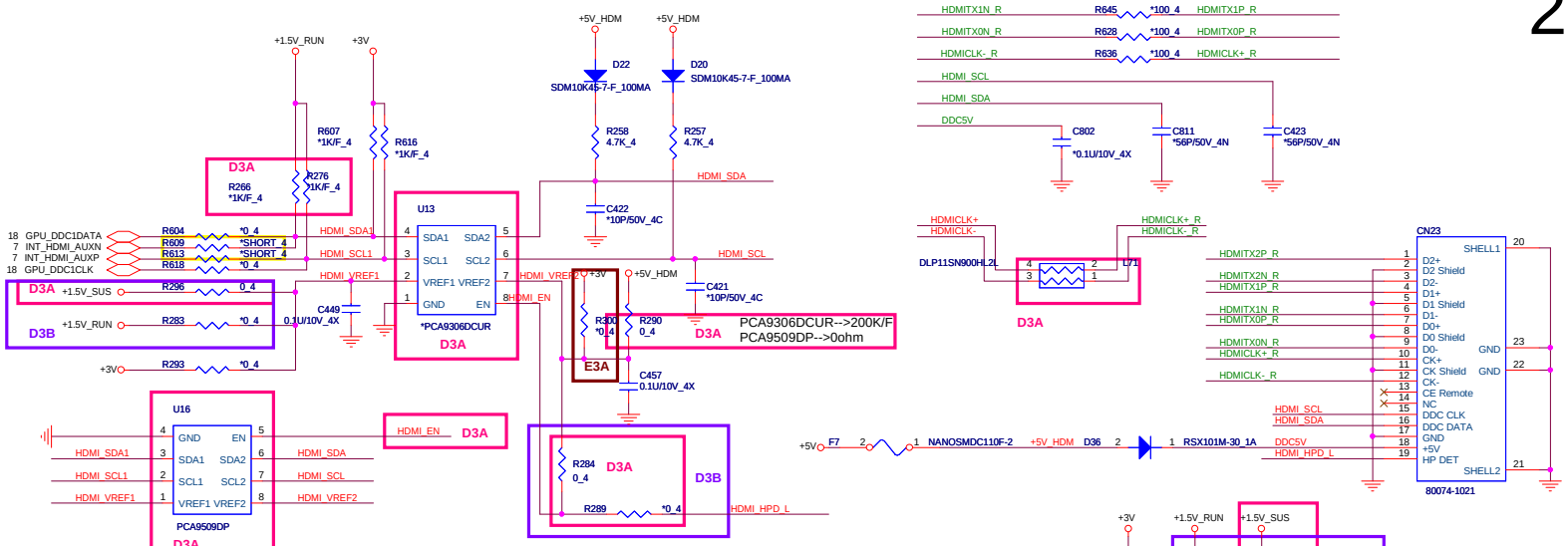
HDMI



HDMI Hot-plug

R316,R311,R335,R330,R343,R339,R327 and R321 need to close to HDMI connector

Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	HDMI	1C
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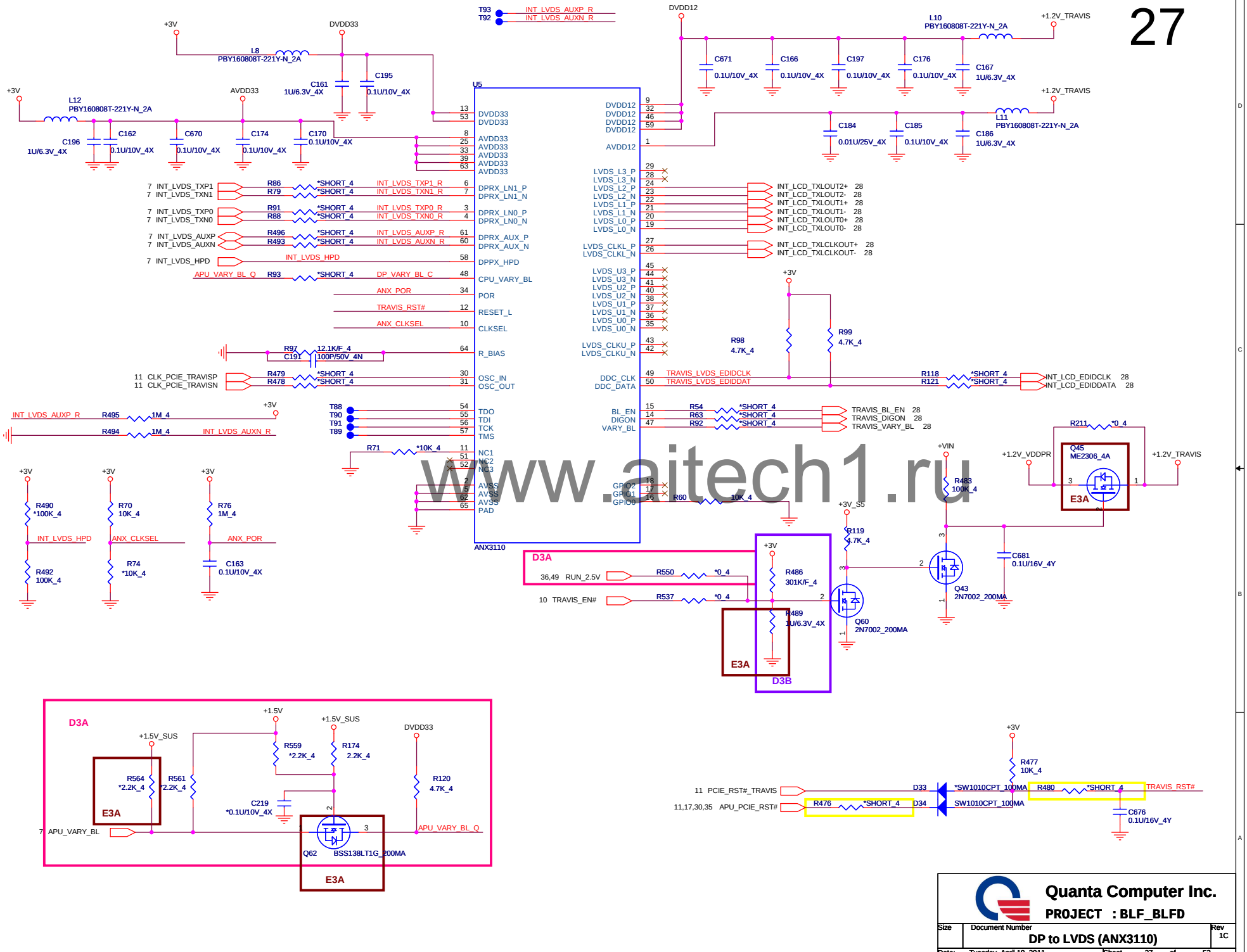
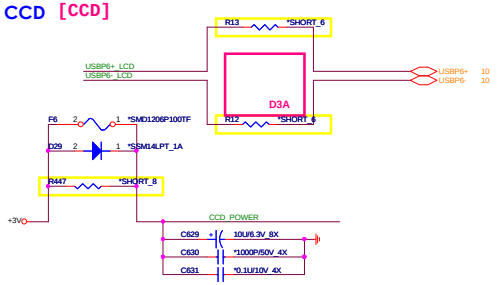
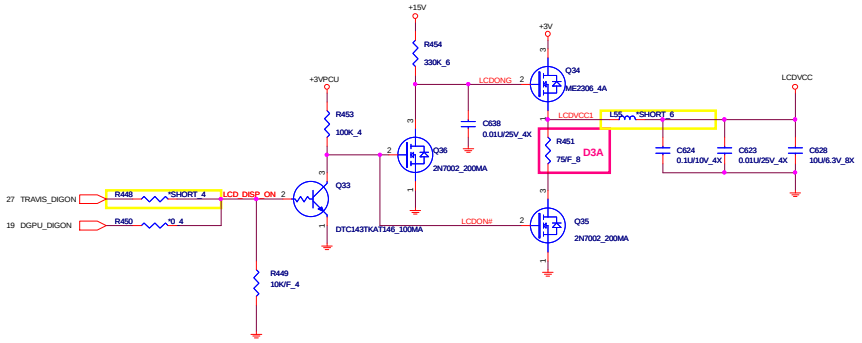


Quanta Computer Inc.		
PROJECT : BLF_BLFD		
Size	Document Number: DP to LVDS (ANX3110)	Rev: 1C
Date: Tuesday, April 19, 2011	Sheet 27 of 53	

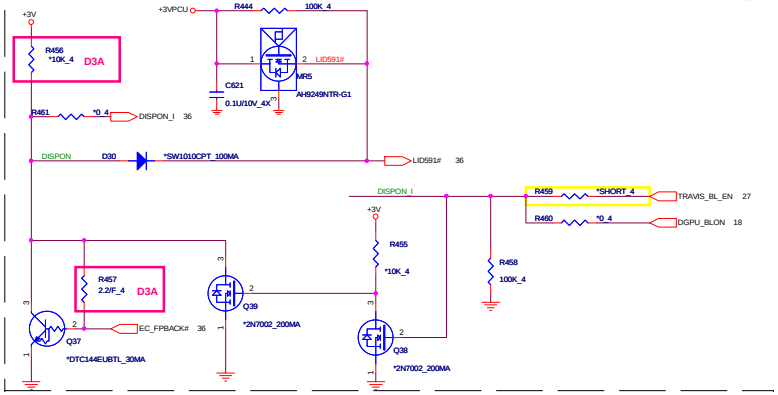
CCD [CCD]



LCD POWER SWITCH [LDS]

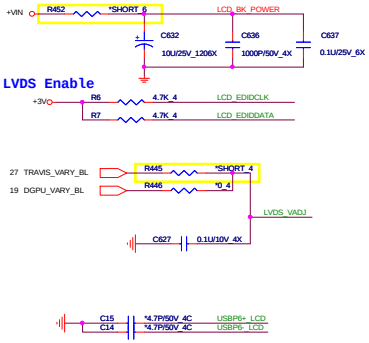


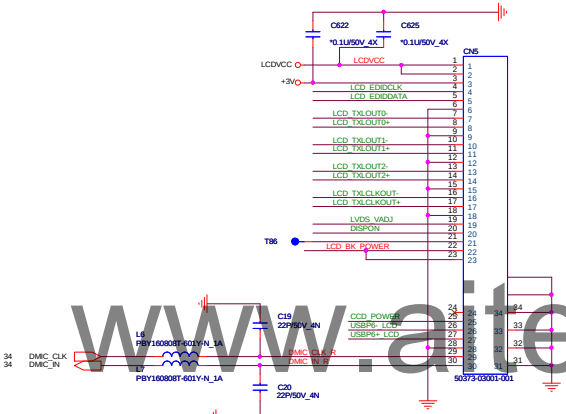
HALL SENSOR&BACK LIGHT SWITCH [HSR]

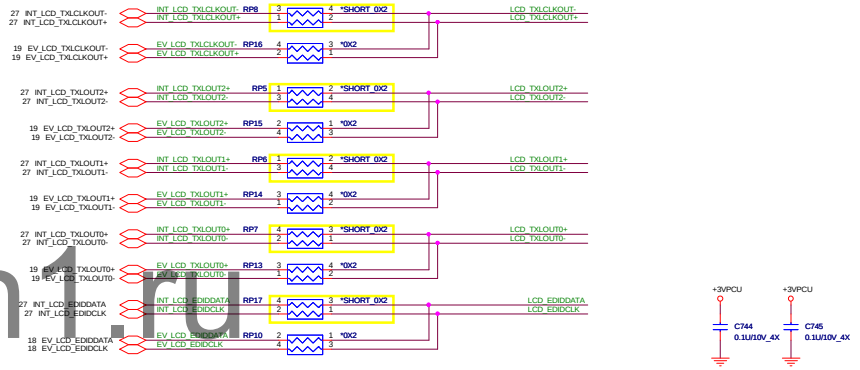


[LDS]

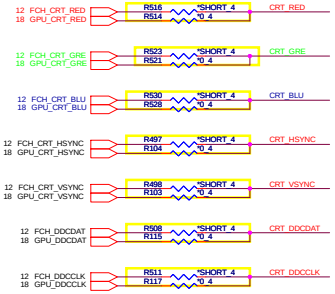
LCD Panel Module

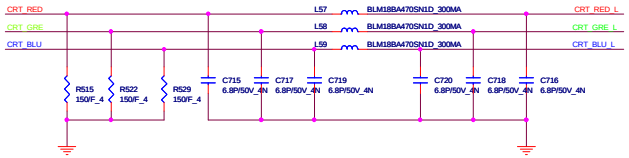


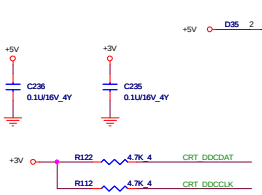


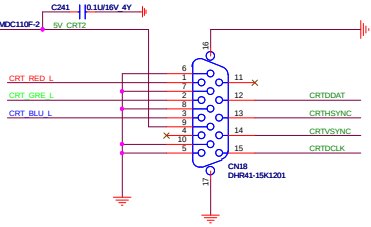


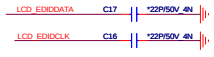
CRT [CRT]

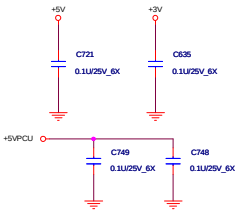


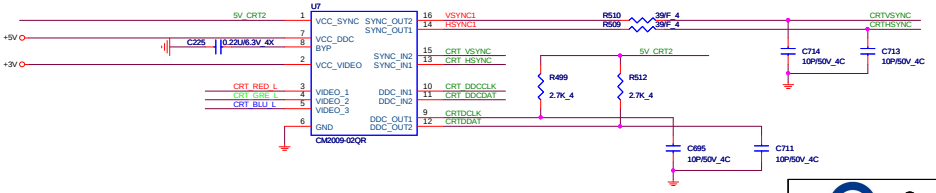












Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	LVDS/CCD/CRT/USB	1C
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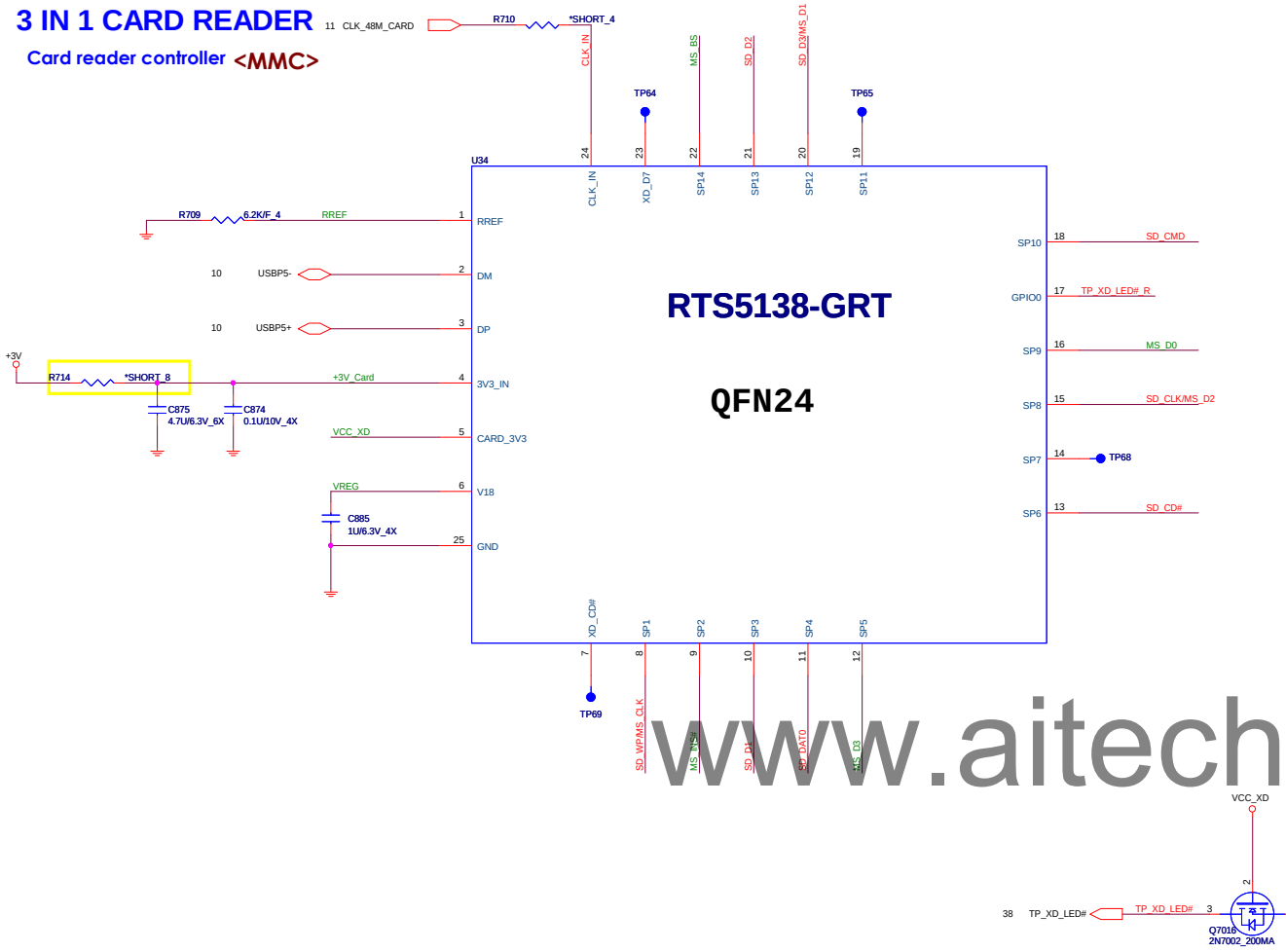
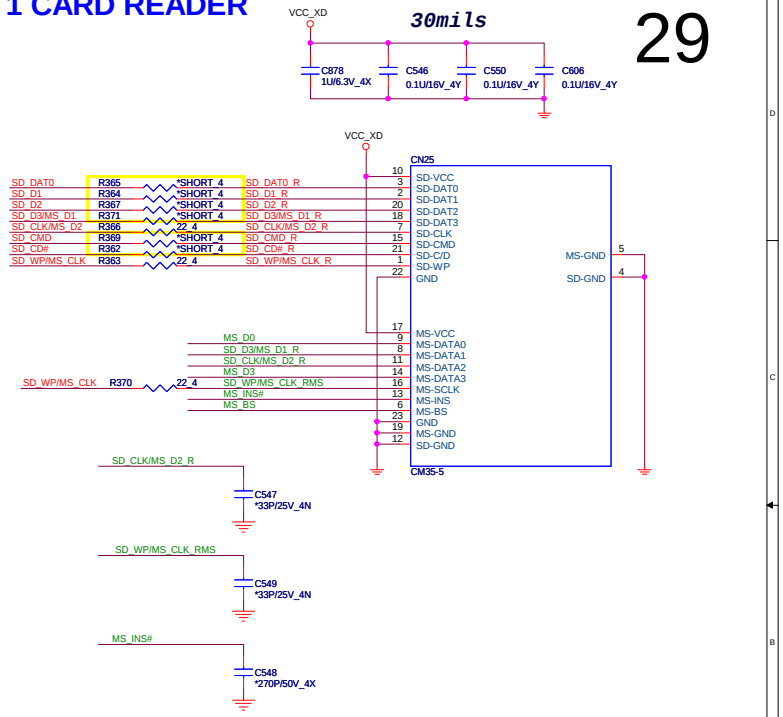
3 IN 1 CARD READER

Card reader controller <MMC>



3 IN 1 CARD READER



Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	RTS5138 (Card Reader)	1C
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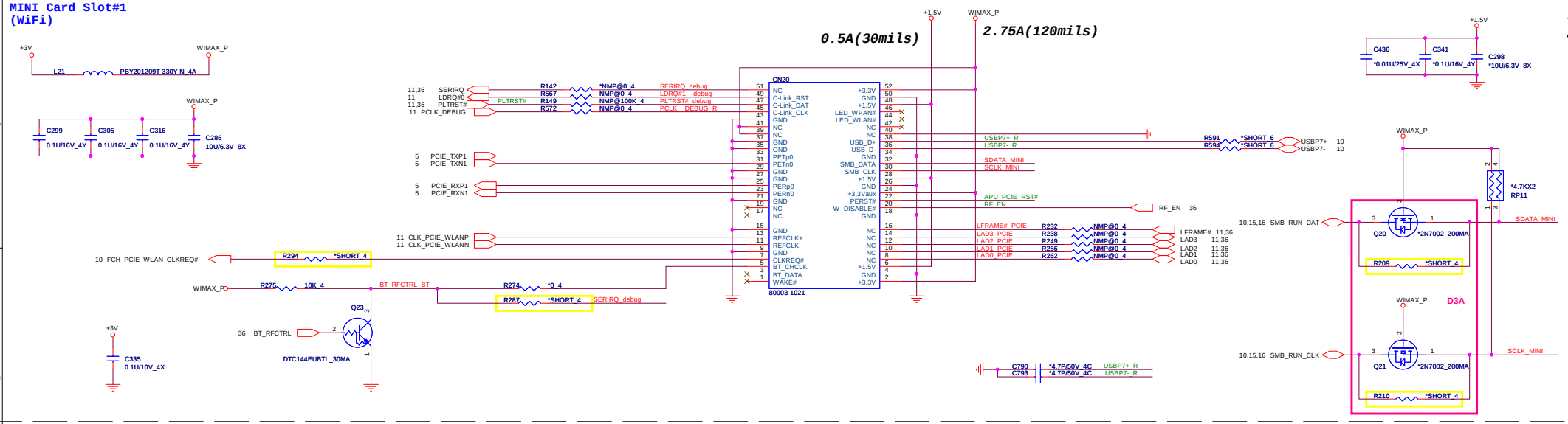
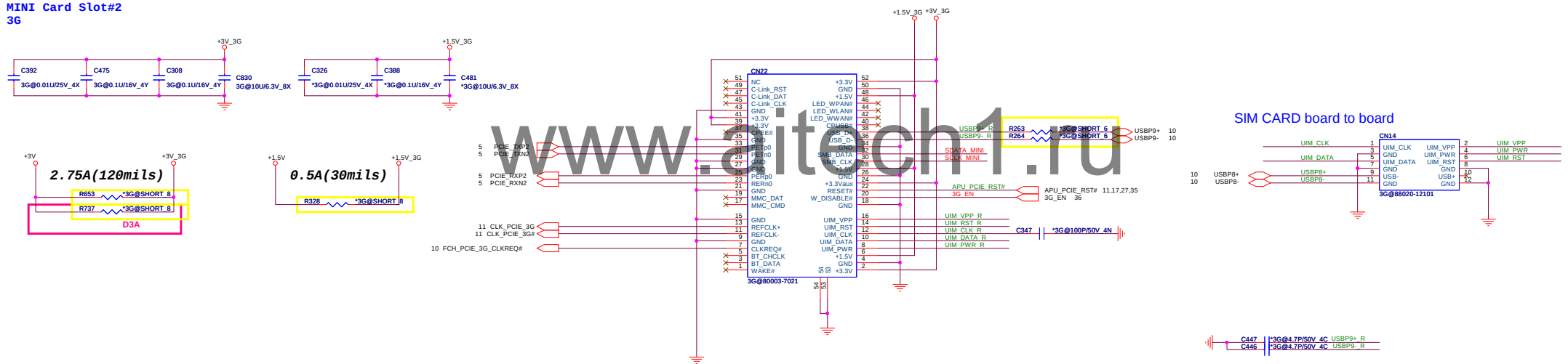
MINI Card Slot#1 (WiFi)



MINI Card Slot#2 3G

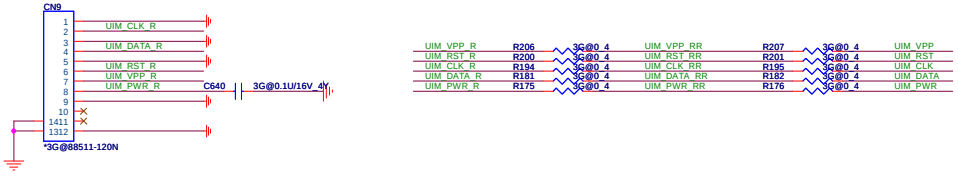


SIM CARD board to board

C447 C446 *3G@4.7P/50V_4C

C634 C633 *3G@4.7P/50V_4C

3G CONN



Quanta Computer Inc.			
PROJECT : BLF_BLFD			
Size	Document Number		Rev
	MINI Card(WLAN/3G/SIM)		1C
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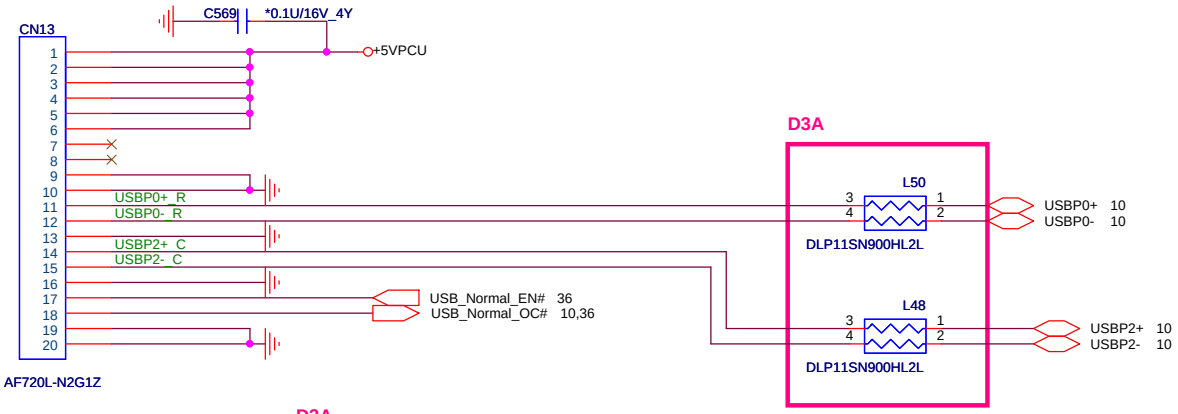
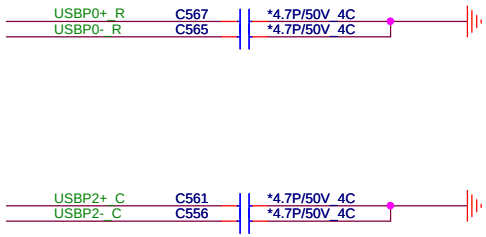
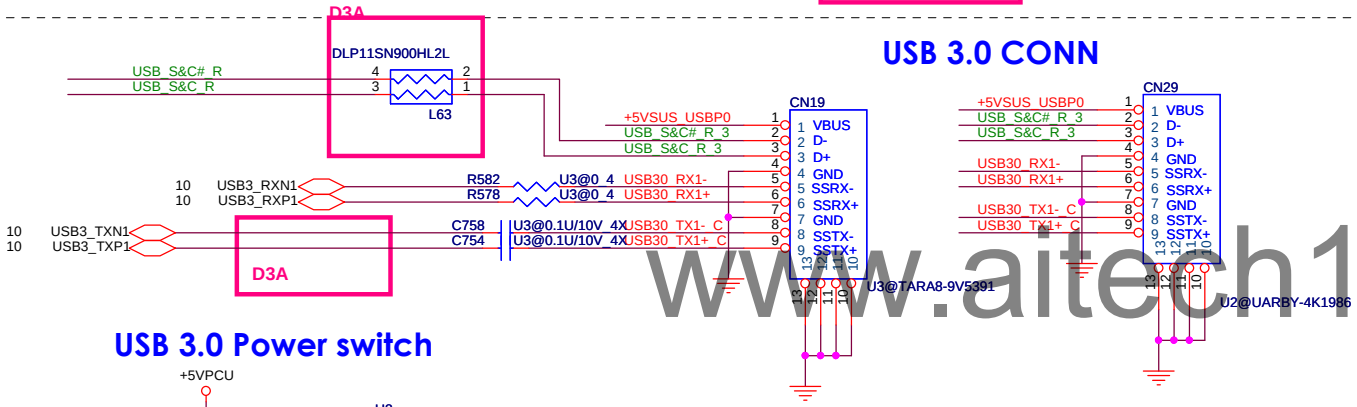
USB board

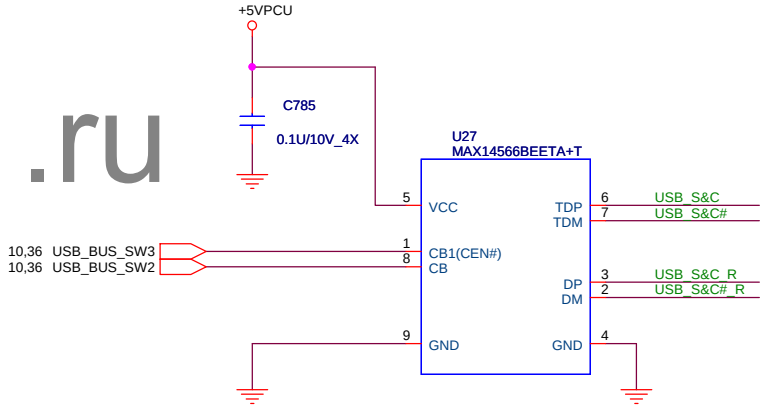




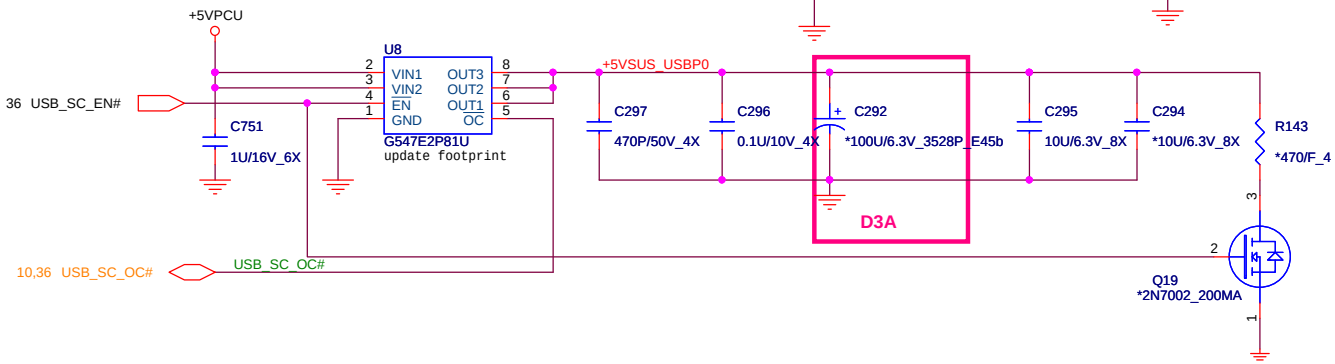
USB 3.0 CONN



USB Sleep & Charge MAXIM solution



USB 3.0 Power switch



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

10 USB_S&C# → USB_S&C#
10 USB_S&C → USB_S&C

Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	USB2.0X1+USB3.0X1	1C
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Quanta Computer Inc.

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	BLANK	1C
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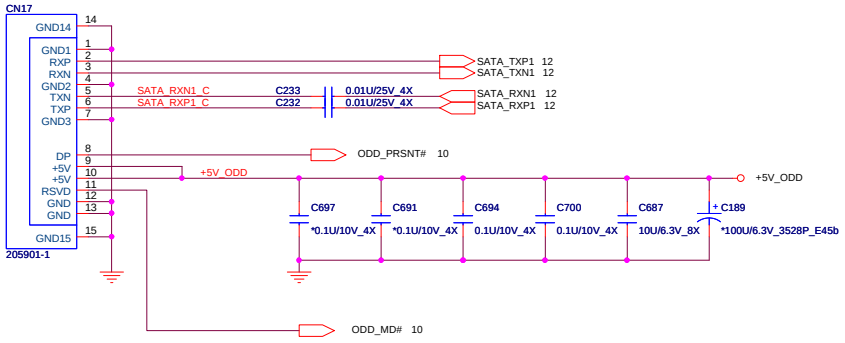
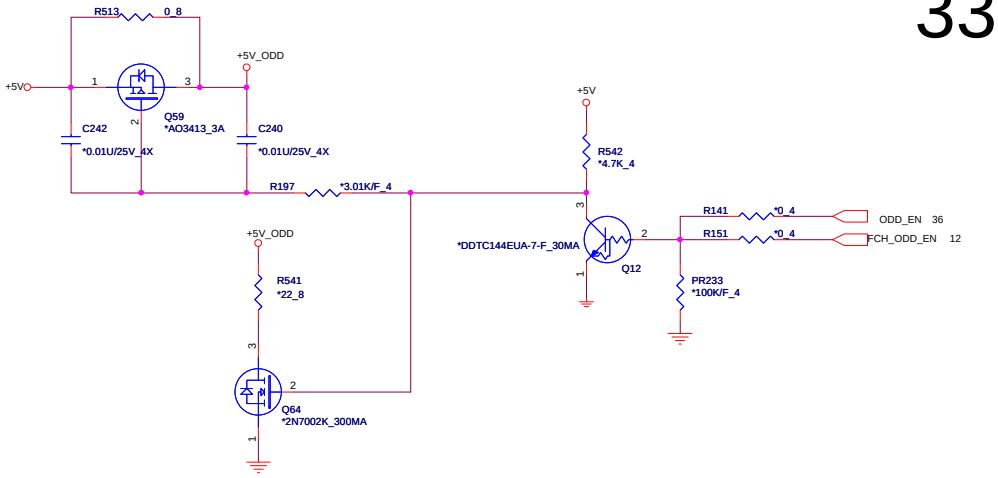
SATA ODD

[ODD]

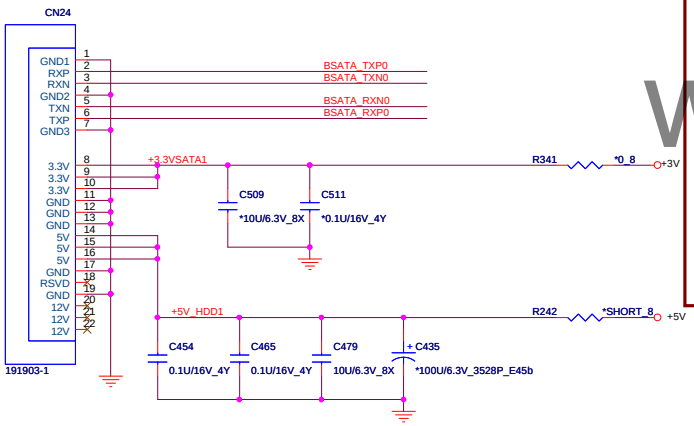


ODD Zero power .

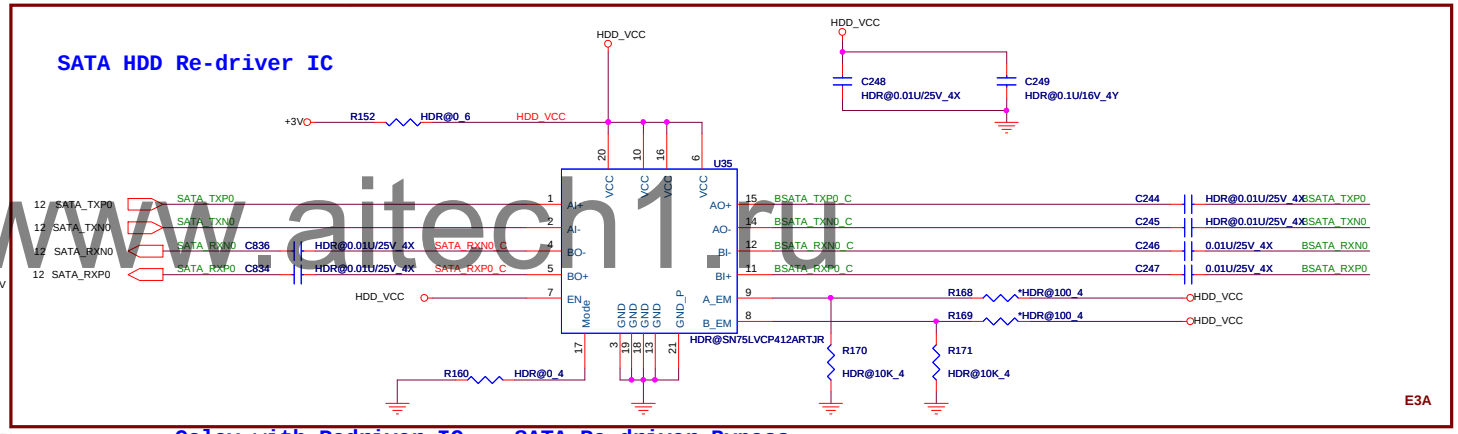


SATA HDD

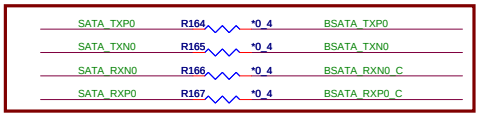
[HDD]



SATA HDD Re-driver IC



Colay with Redriver IC SATA Re-driver Bypass



Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	HDD/ODD/MDC	1C

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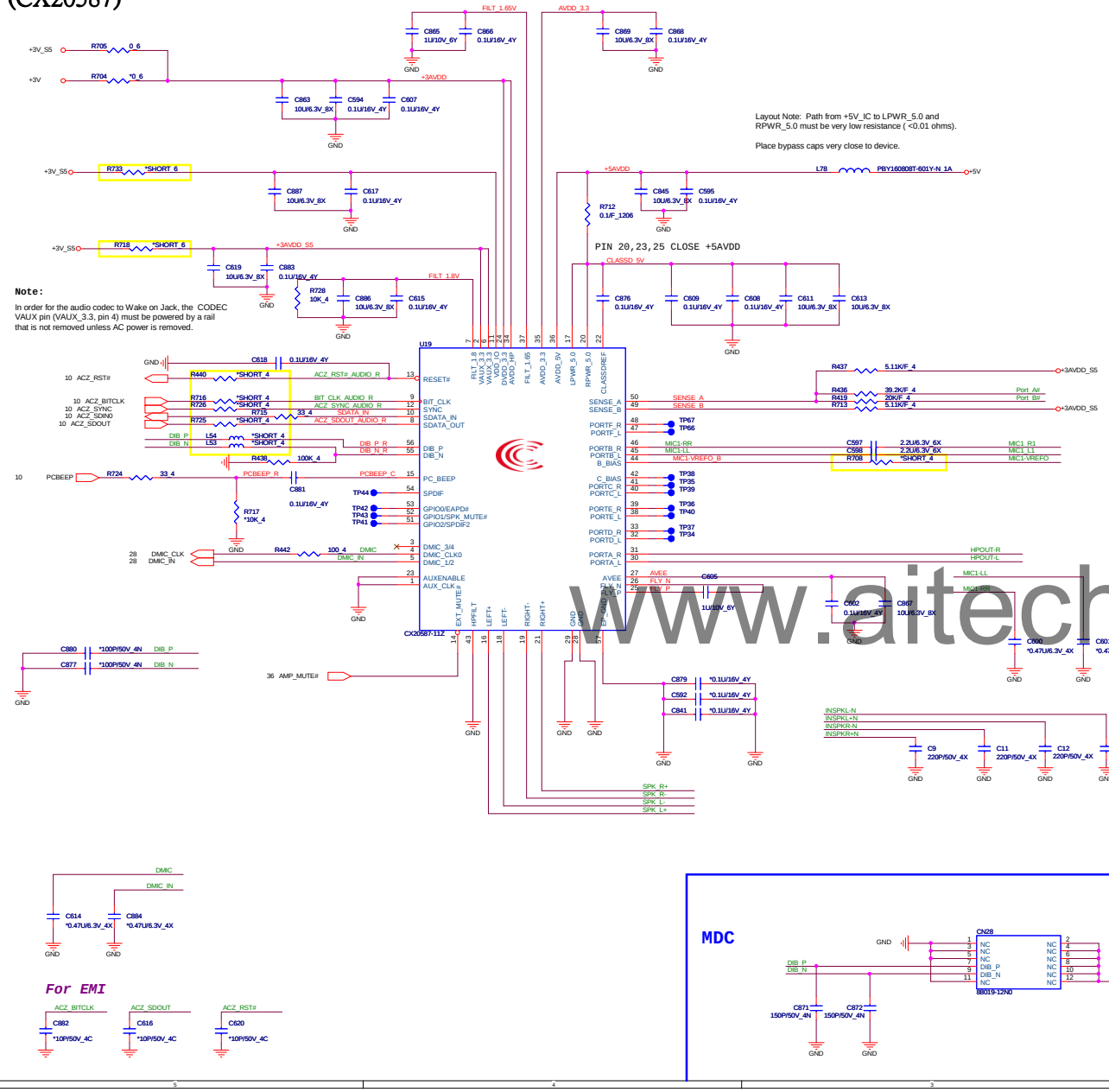
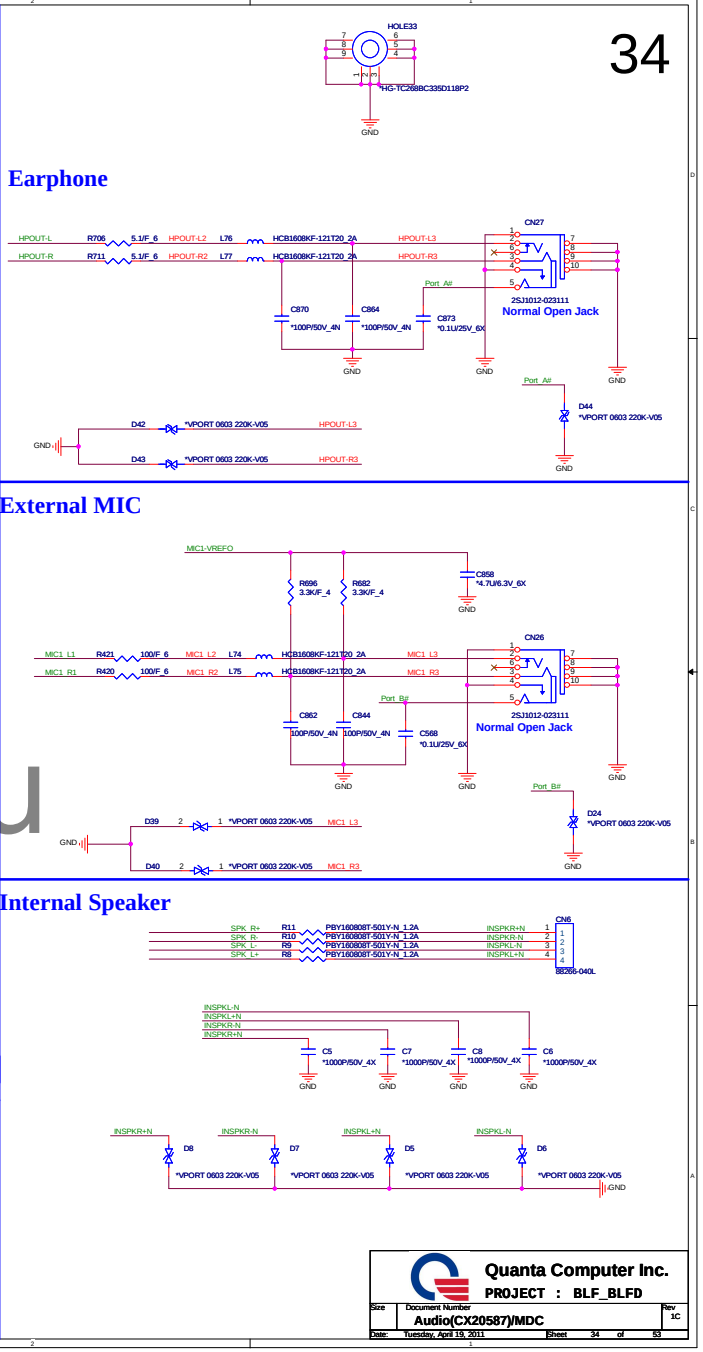
Codec (CX20587)





Quanta Computer Inc.
PROJECT : BLF_BLFD
Size | Document Number: Audio(CX20587)/MDC | Rev: 1C
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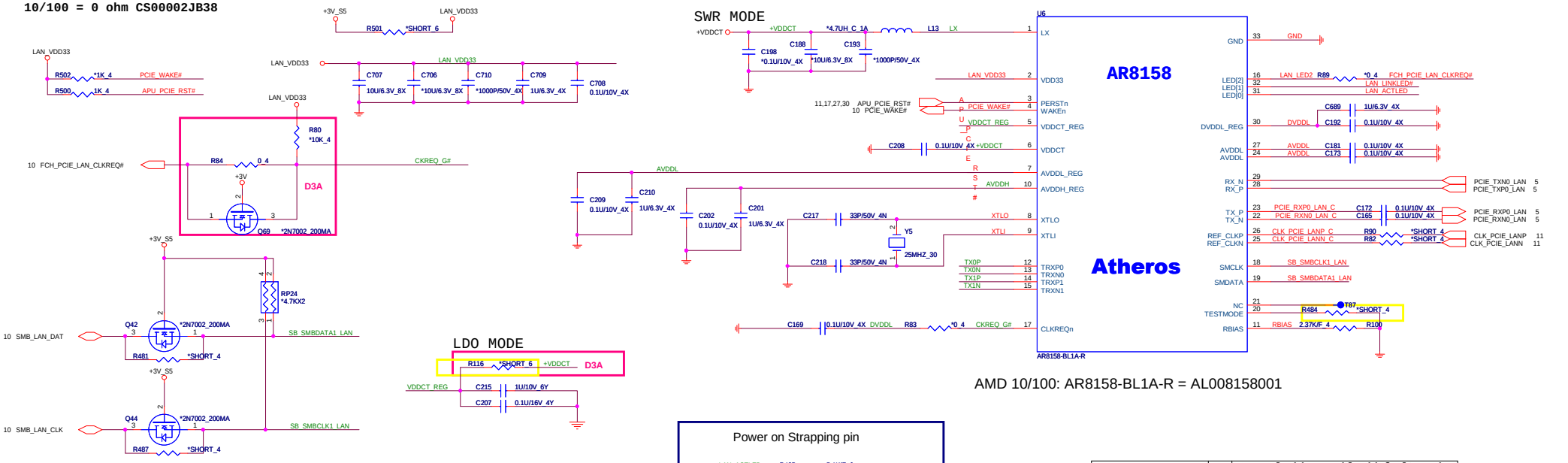
Atheros Lan AR8158

10/100 = 0 ohm CS00002JB38



AMD 10/100: AR8158-BL1A-R = AL008158001

LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low

14" RJ45- DFTJ08FR164
15" RJ45- DFTJ08FR169
Transformer- DB0EL5LAN02

Quanta Computer Inc.
PROJECT : BLF_BLFD

Size	Document Number	Rev
	Atheros LAN(AR8158)	1C
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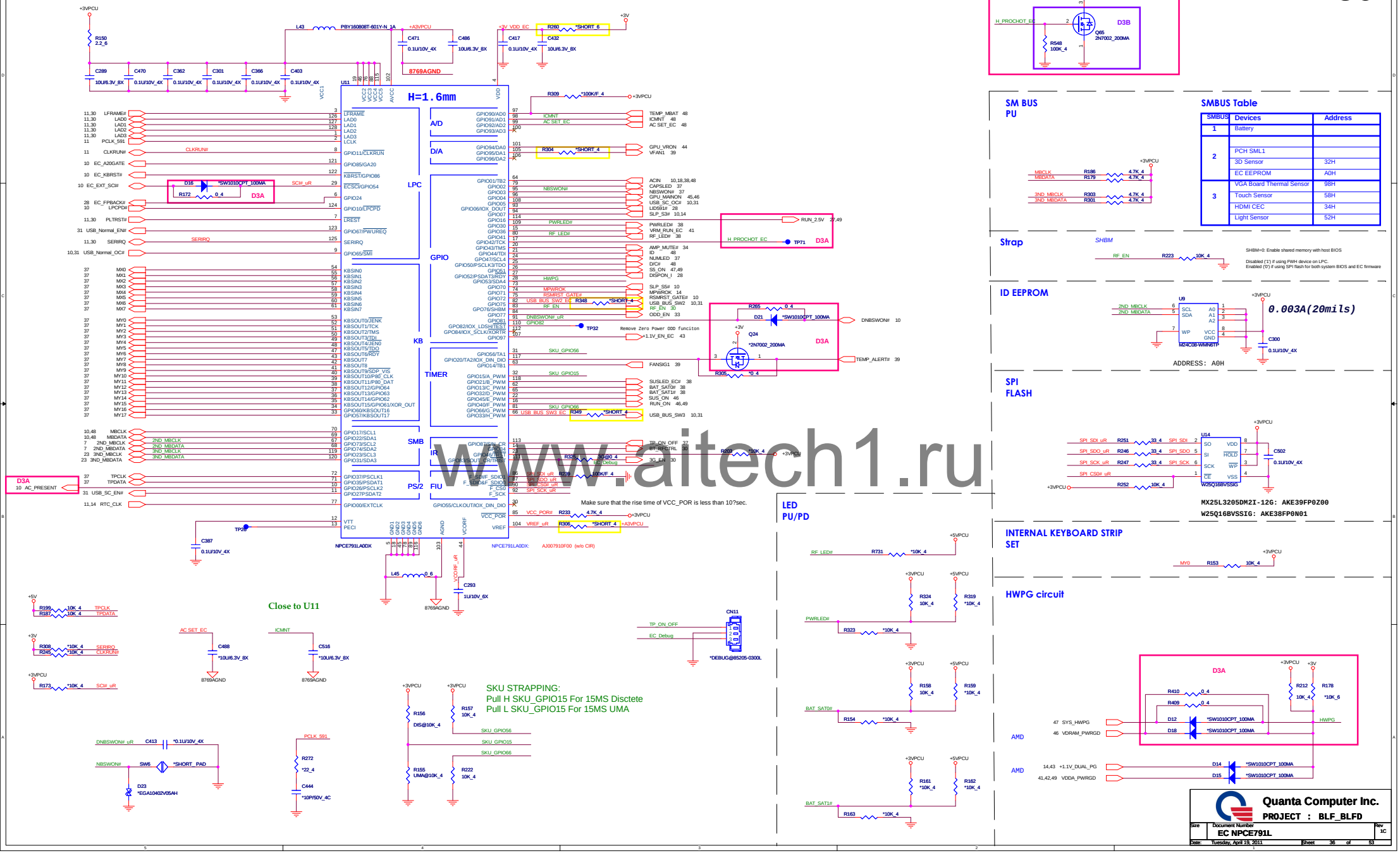
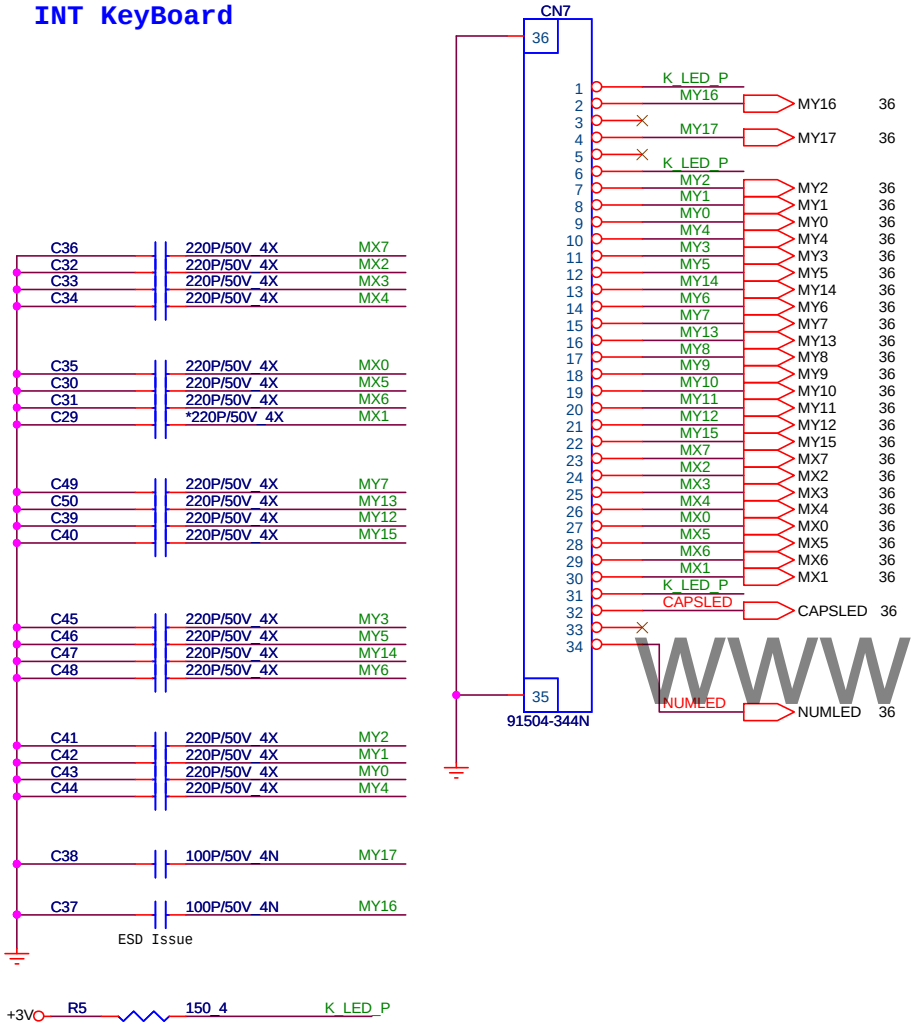
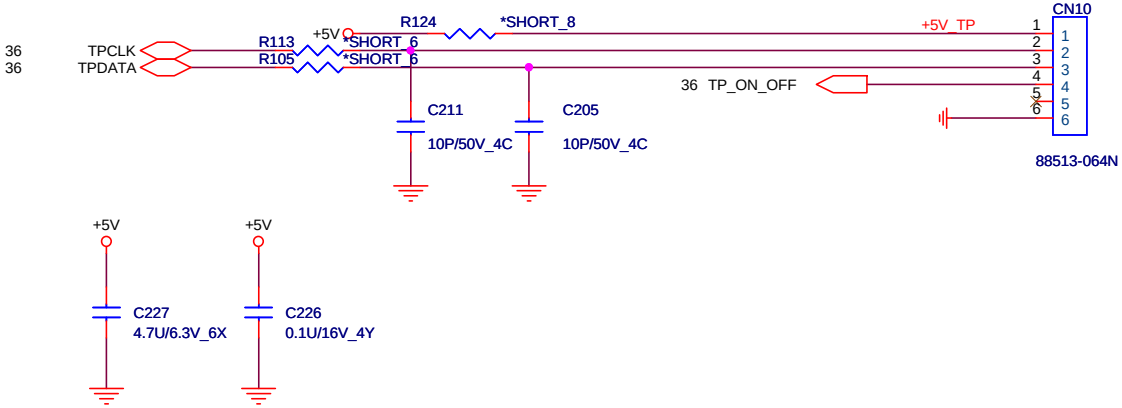


KEY BOARD Connector

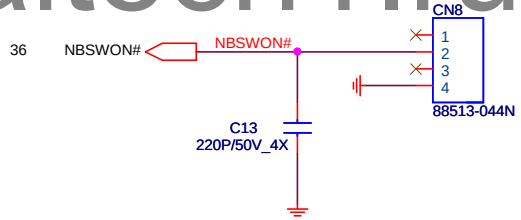
INT KeyBoard



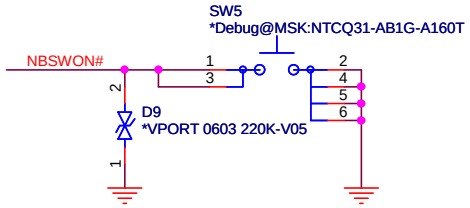
TOUCH PAD BOARD



Power Board (UIF)



Power Switch (debug only)



Quanta Computer Inc.

PROJECT : BLF_BLFD

Size	Document Number	Rev
	FP/TP/KB Conn	1C
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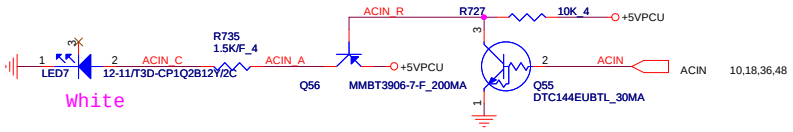
LED

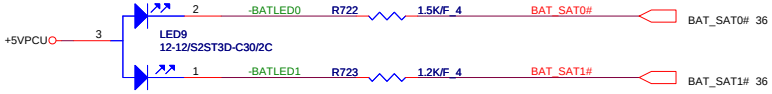
AC-IN



White

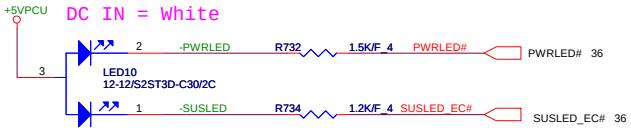
BATERRY

Full Charge = White



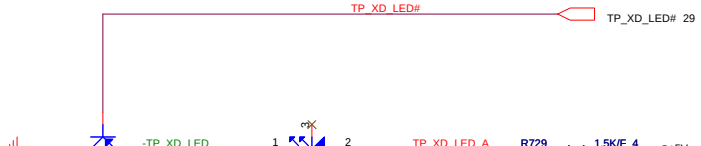
Charging = Orange

POWER



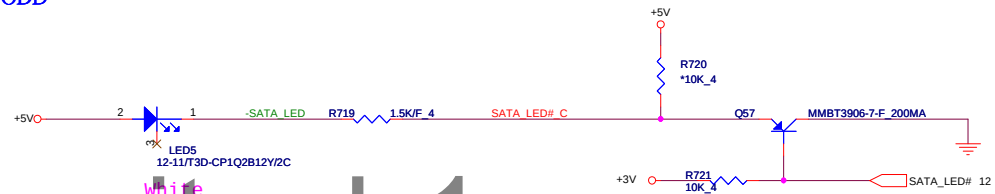
S3 Mode = Orange

CARDREADER



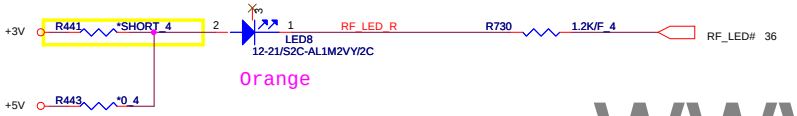
White

HDD/ODD



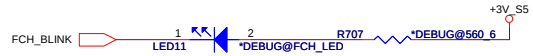
White

RF LED

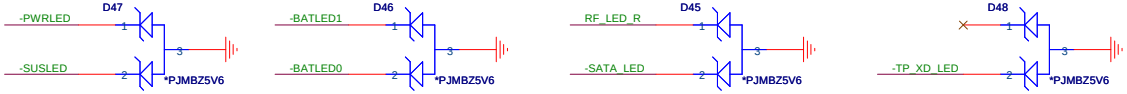


Orange

When ON, means in S0
When BLINK, means in S3
When OFF, means in S5



Orange



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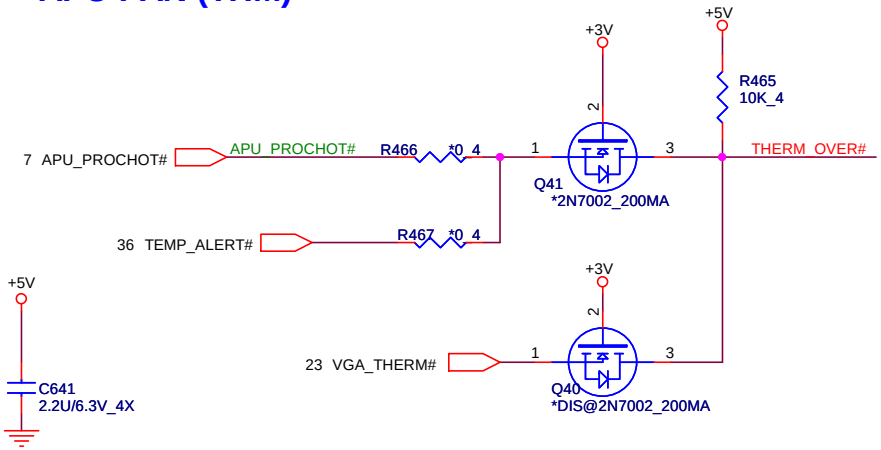
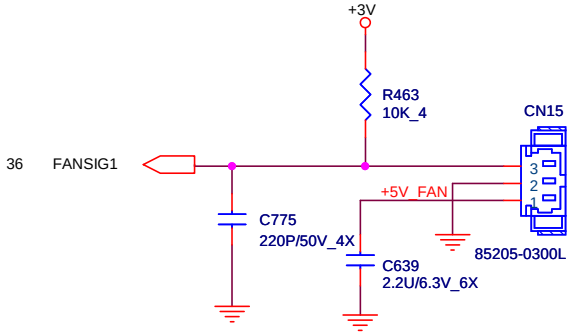
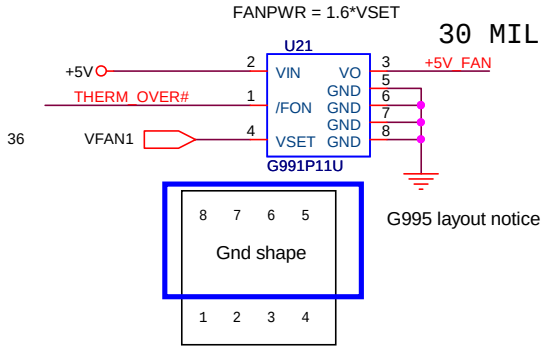
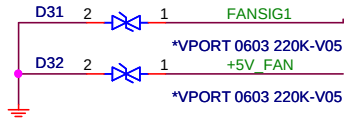
APU FAN (THM)









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Size	Document Number	Rev
	APU FAN	1C

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Quanta Computer Inc.		
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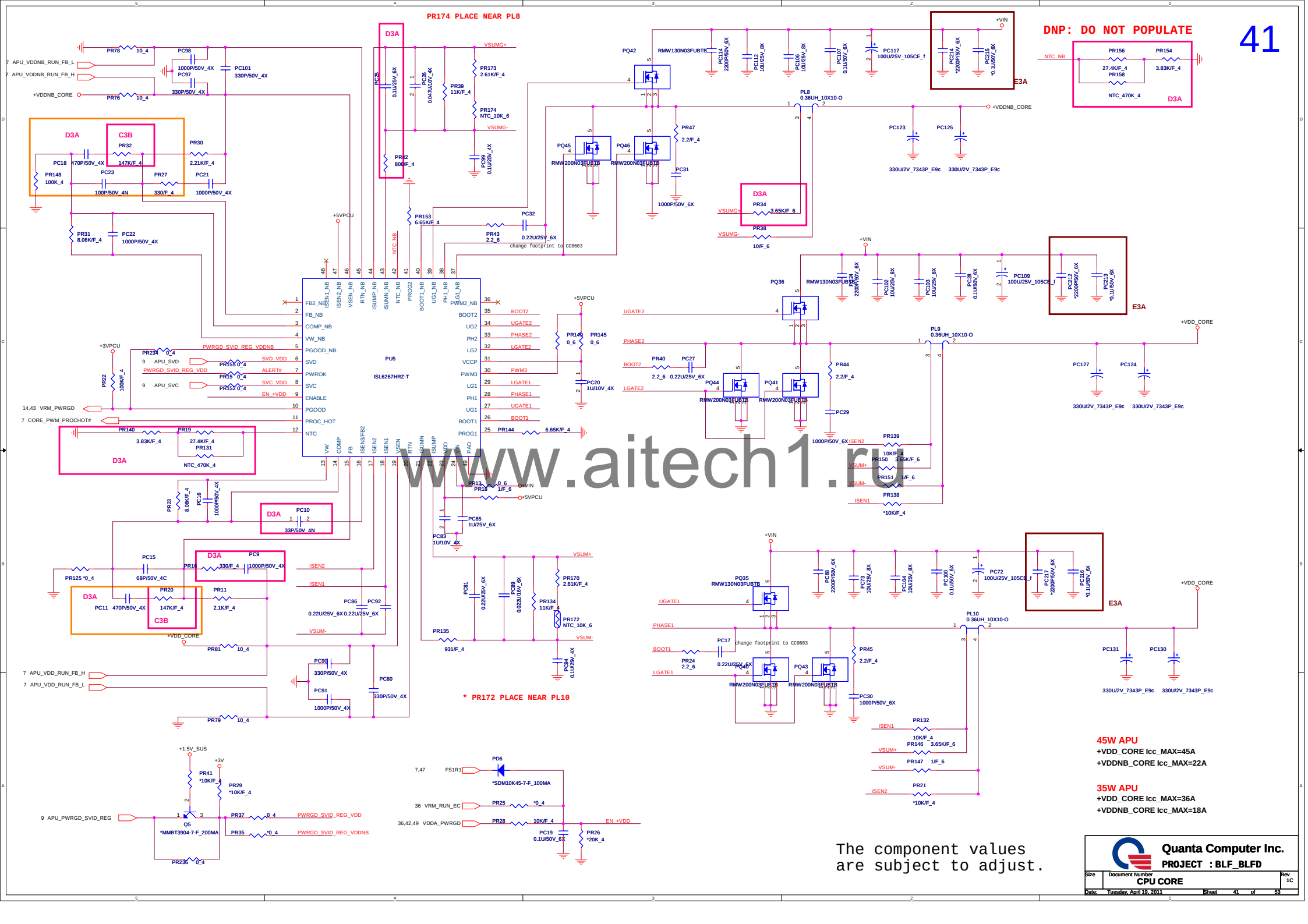
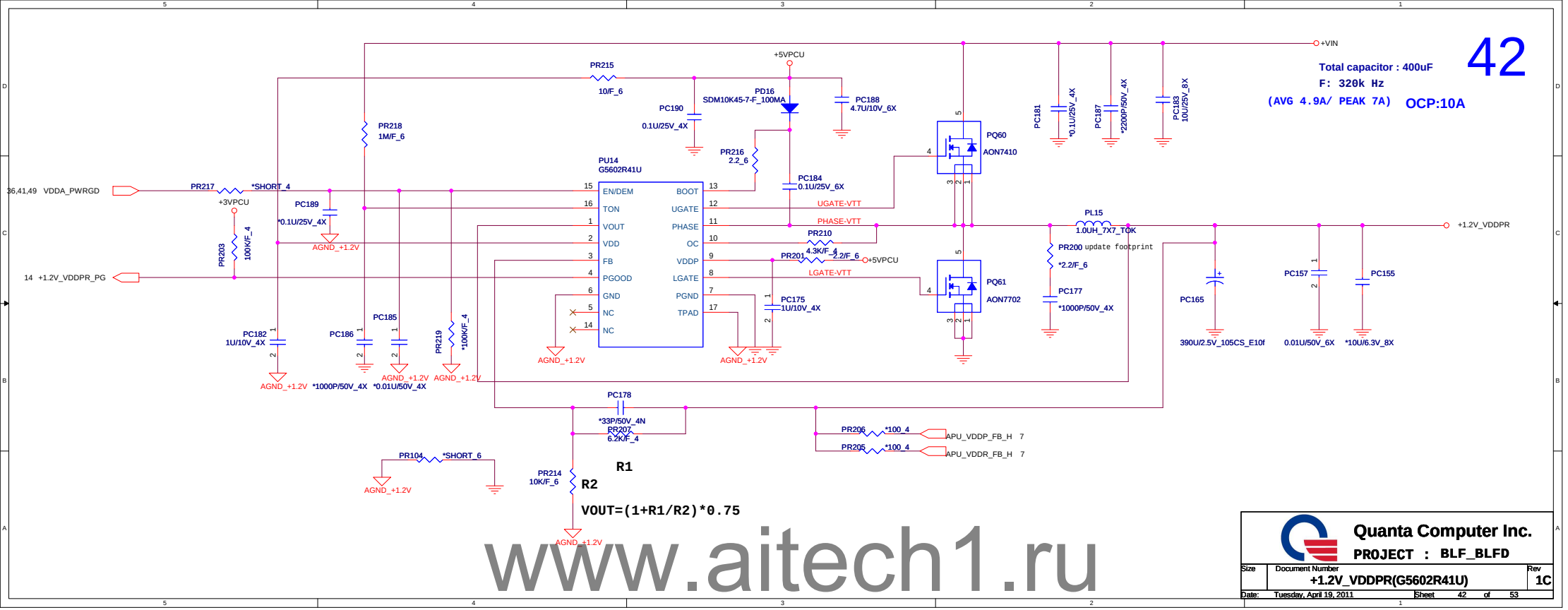
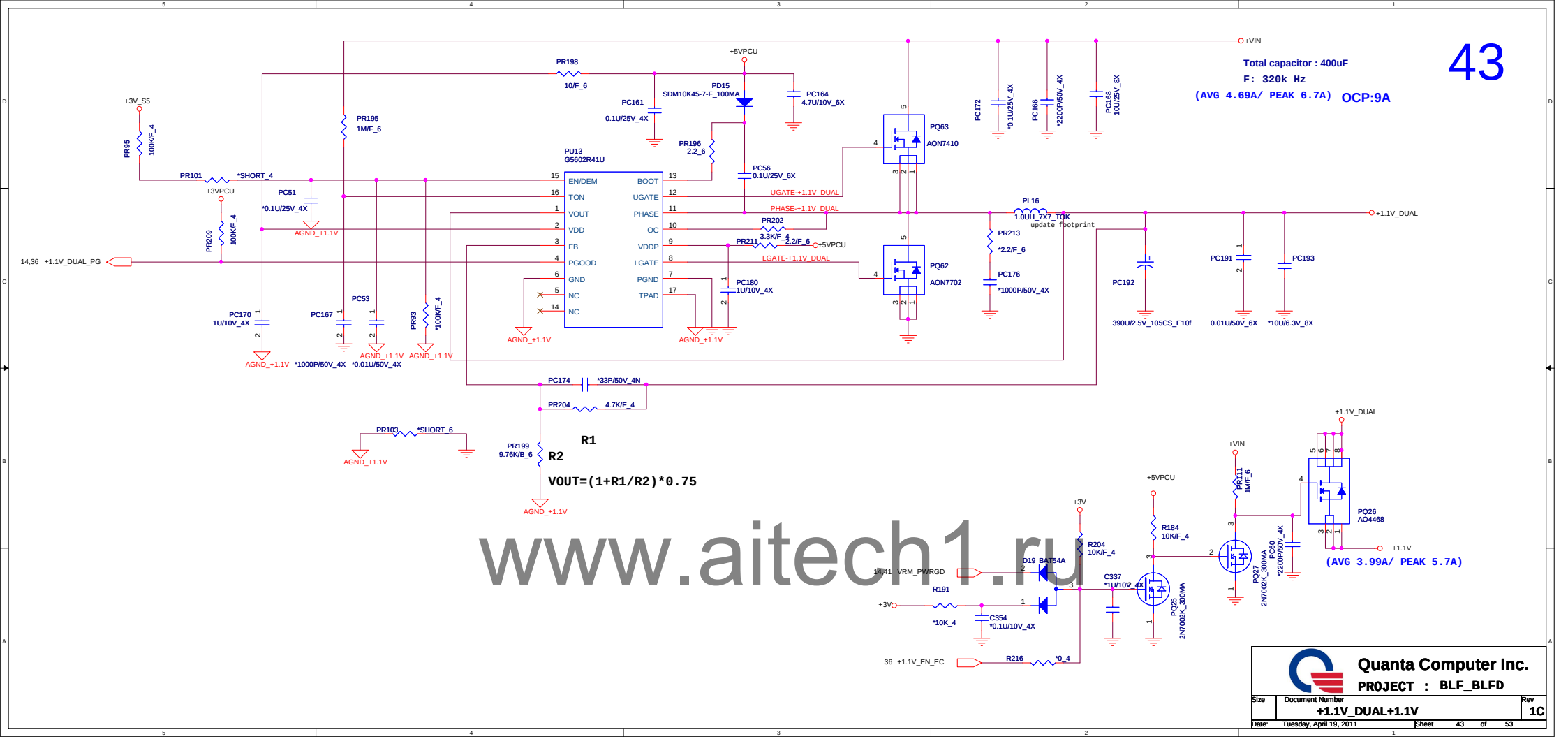
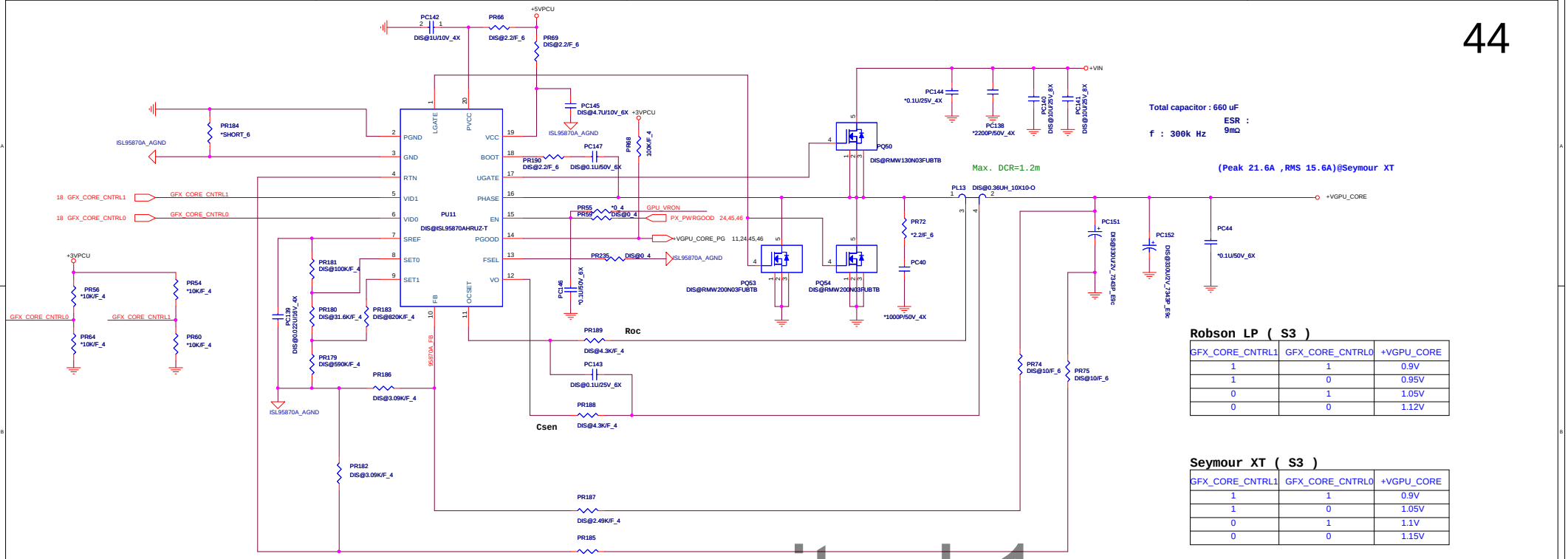

PR174 PLACE NEAR PL8
DNP: DO NOT POPULATE
41
ISL6267HRZ-T
PU5
* PR172 PLACE NEAR PL10
45W APU
+VDD_CORE Icc_MAX=45A
+VDDNB_CORE Icc_MAX=22A
35W APU
+VDD_CORE Icc_MAX=36A
+VDDNB_CORE Icc_MAX=18A
The component values are subject to adjust.
Quanta Computer Inc.
PROJECT : BLF_BLFD
CPU CORE
Tuesday, April 19, 2011
www.aitech1.ru





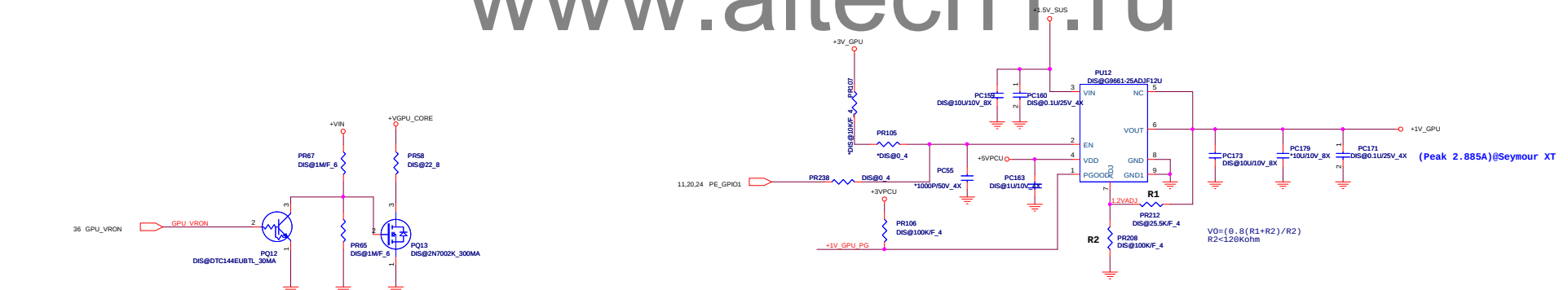


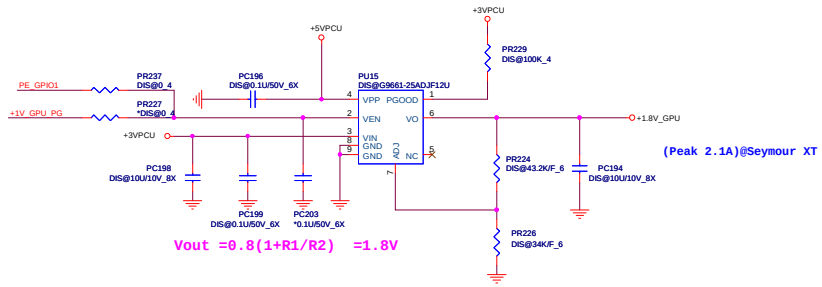
Robson LP (S3)

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.12V

Seymour XT (S3)

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	1.05V
0	1	1.1V
0	0	1.15V





PCIE_VDDC

Madison,Park-->1.0V

	Madison,Park
R1	25.5K/F_4 (CS32552FB11)
R2	100K/F_4 (CS41002FB28)

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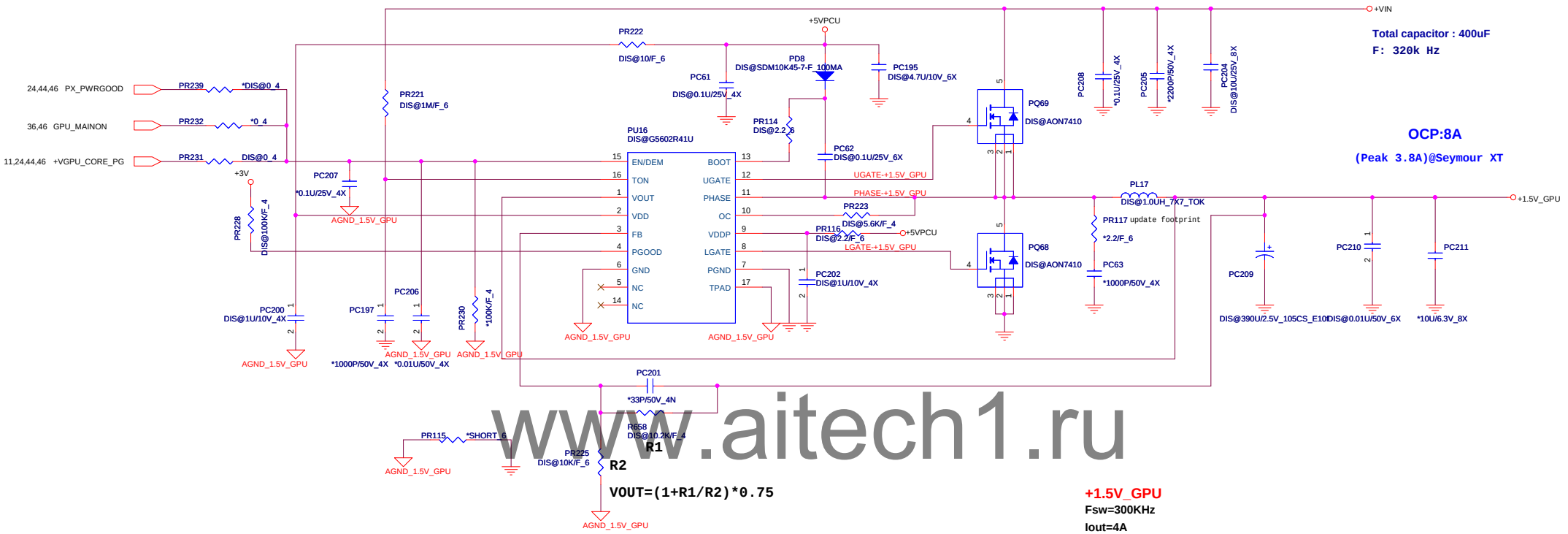

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(Peak 0.5A, AVG 0.35A)

(Peak 0.1A, AVG 0.07A)

RT8207LGQW
PU9
FOR DDR III

RDSon=2.3m ohm

OCP:16A
(Peak 13.72A, AVG 10.129A)
ESR : 9mΩ
f : 400k Hz

For RT8207A 400KHZ

Vout = (R1/R2) X 0.75 + 0.75

MEM_P1V5	MEM_P1V35	+1.5VSUS
1	DONT CARE	1.50V
0	1	1.35V
0	0	1.25V

(Peak 2.8A ,RMS 2.3A)
(Peak 6.4A ,RMS 4.4A)

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Size	Document Number	Rev
	DDR1.5V(RT8207LGQW)	1C

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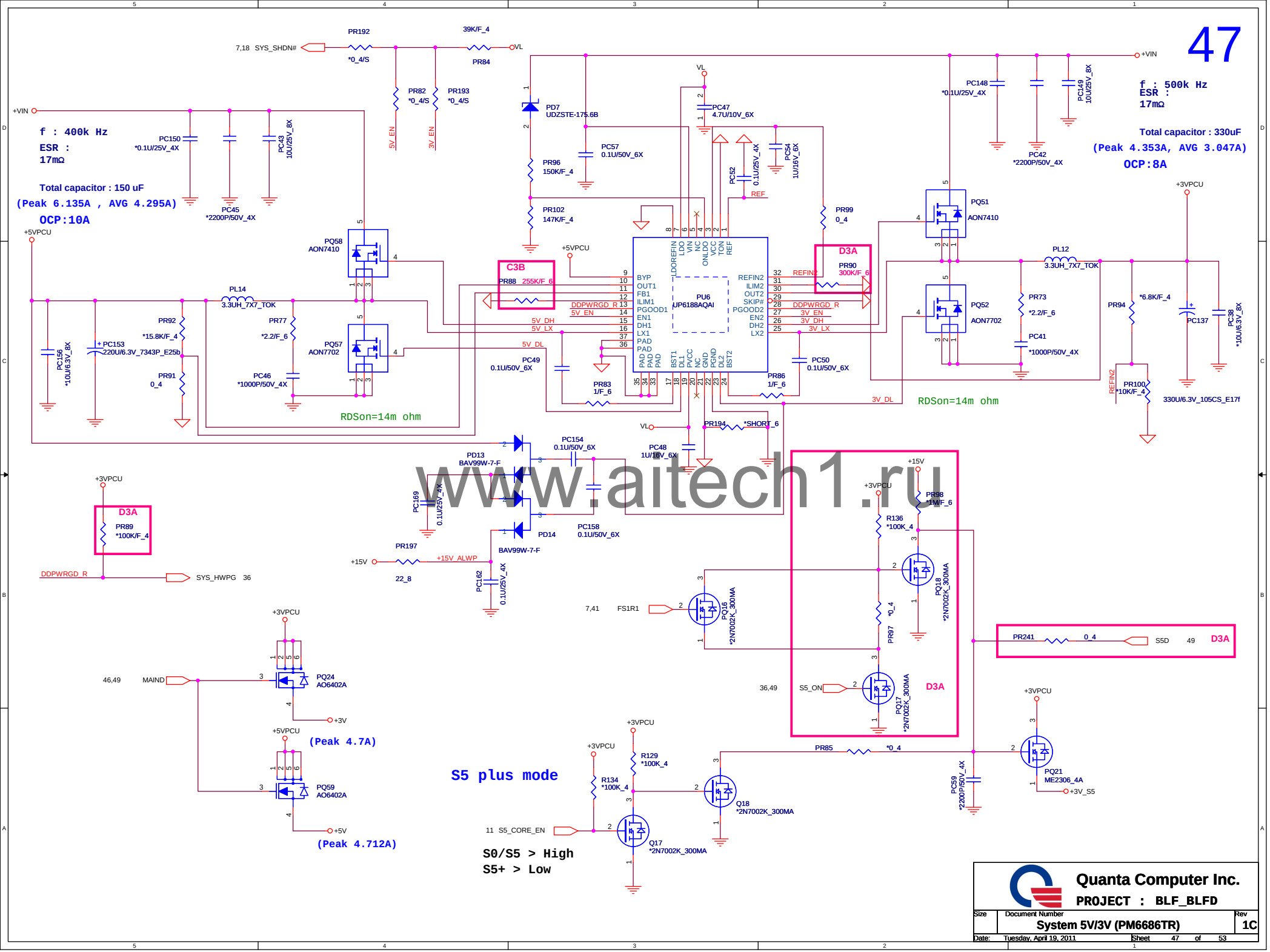

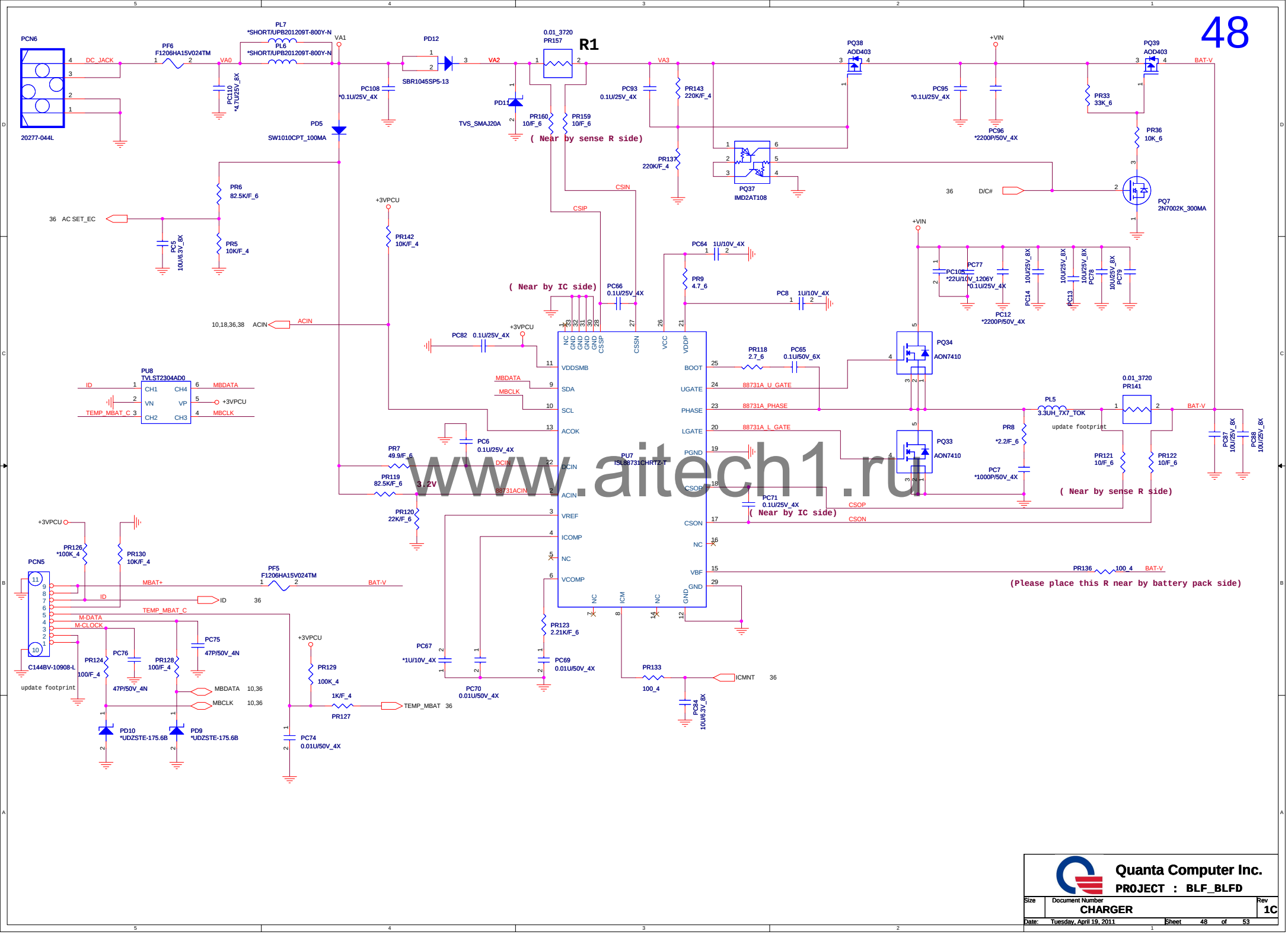

Quanta Computer Inc.
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	CHARGER	1C
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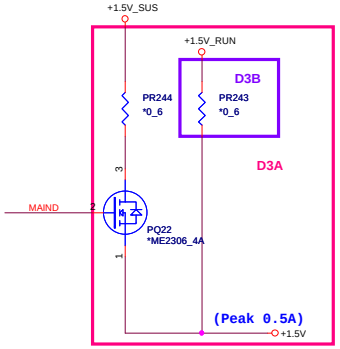
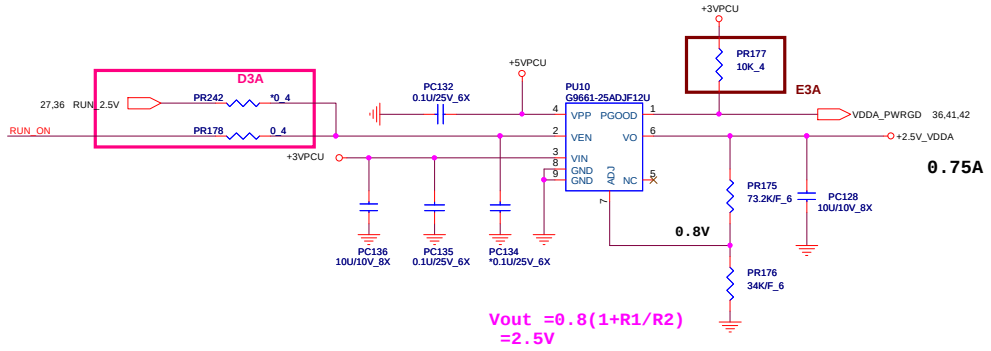
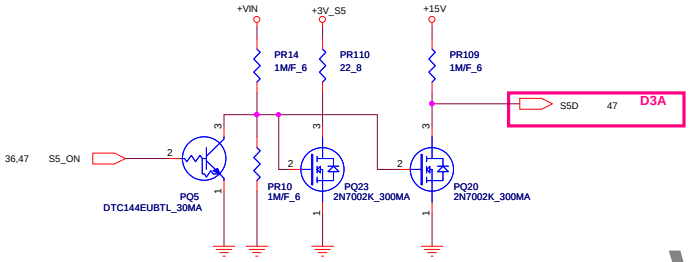
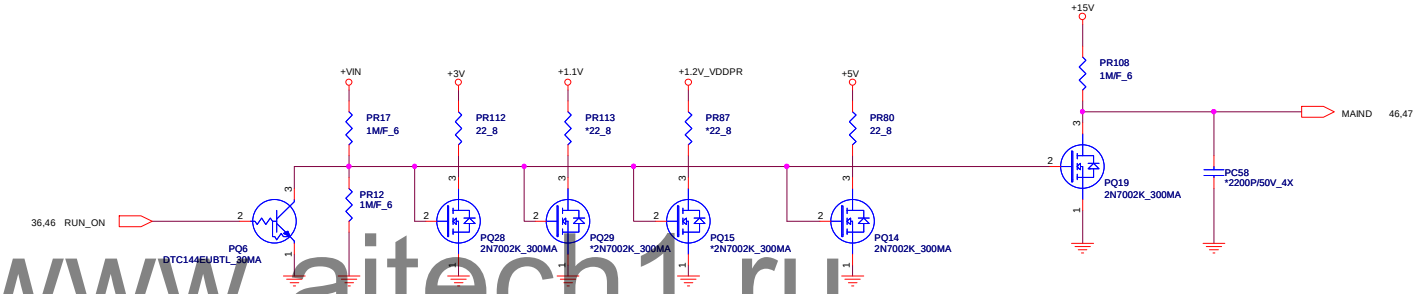


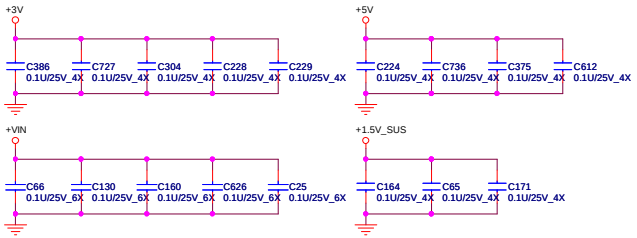


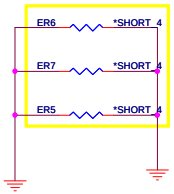


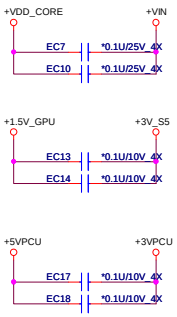


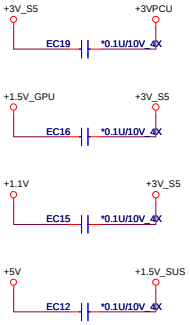
EMI

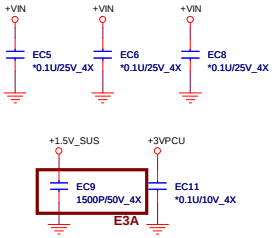
For EMI











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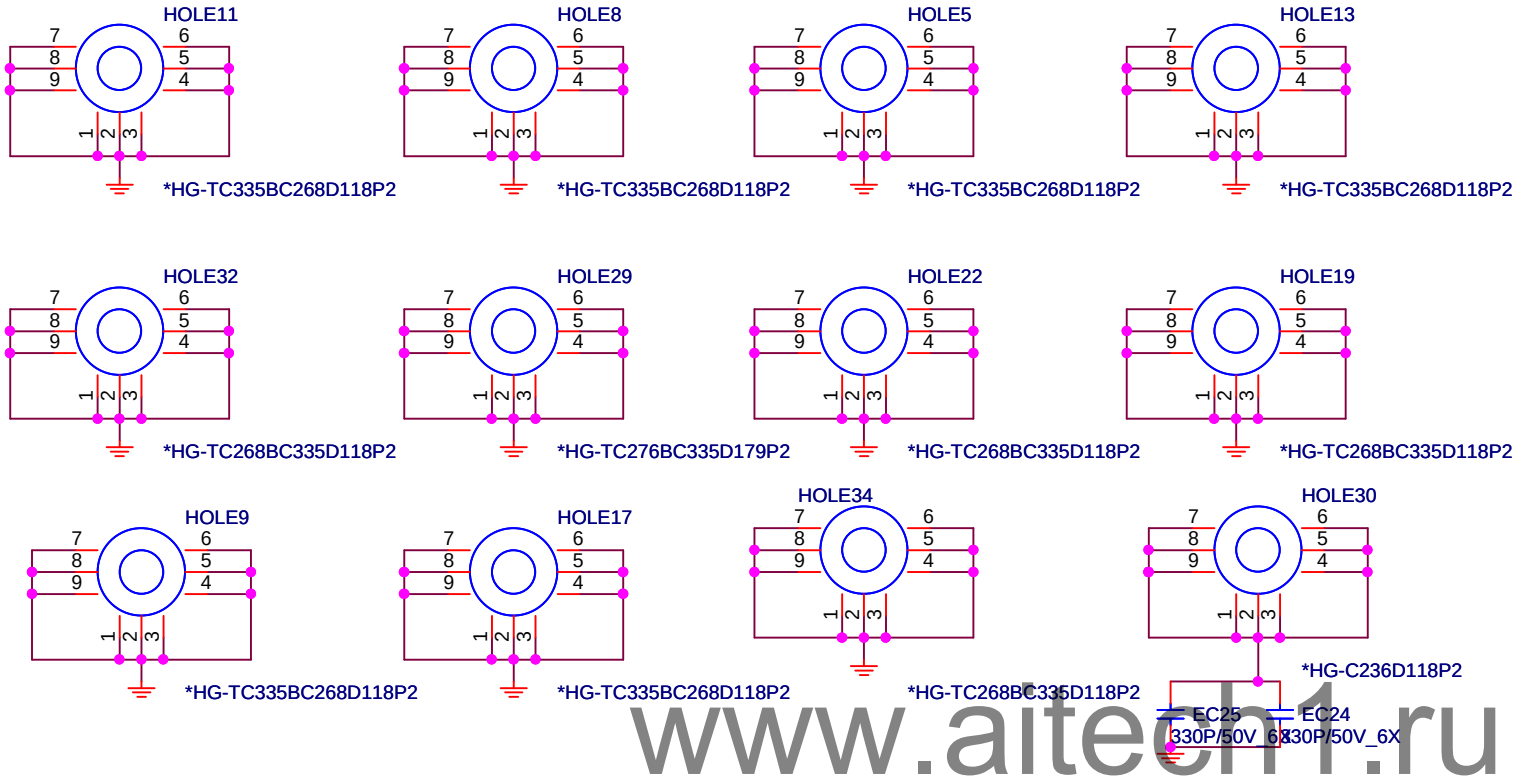

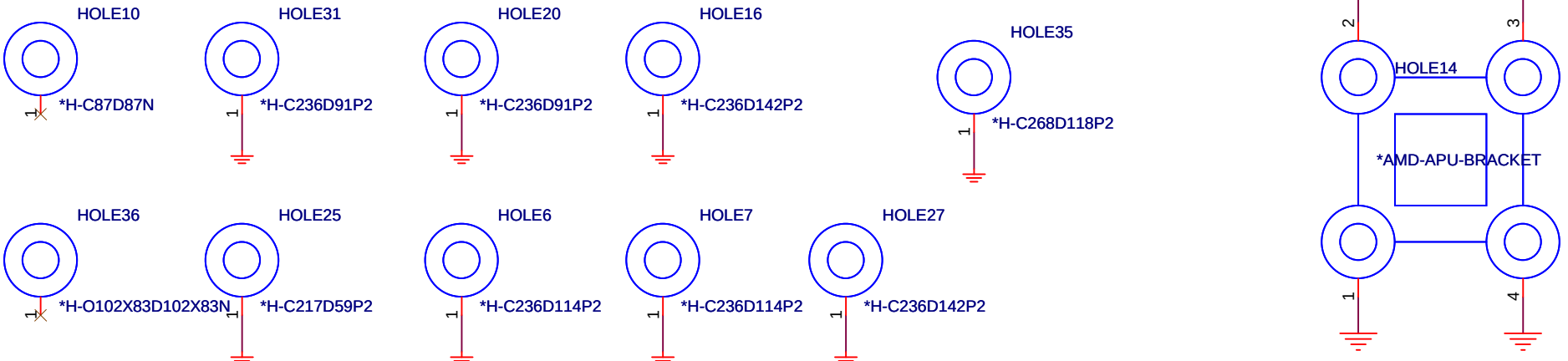

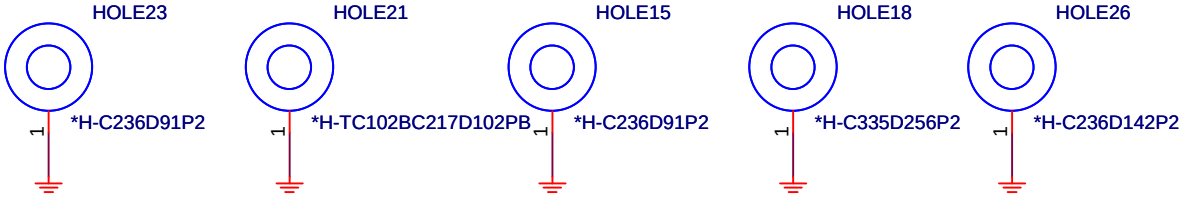

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	Screw	1C
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